

FIG. 2

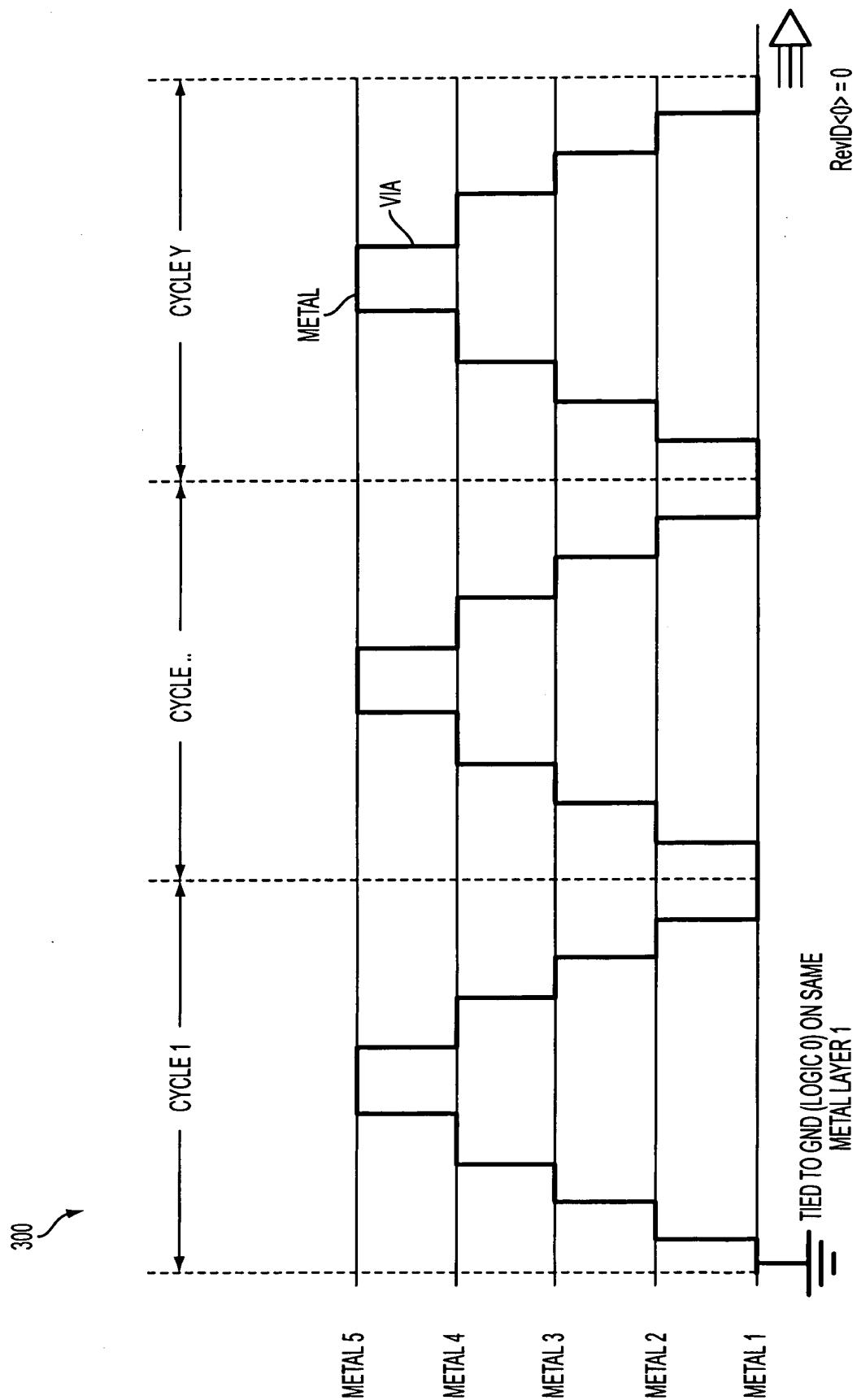


FIG. 3A

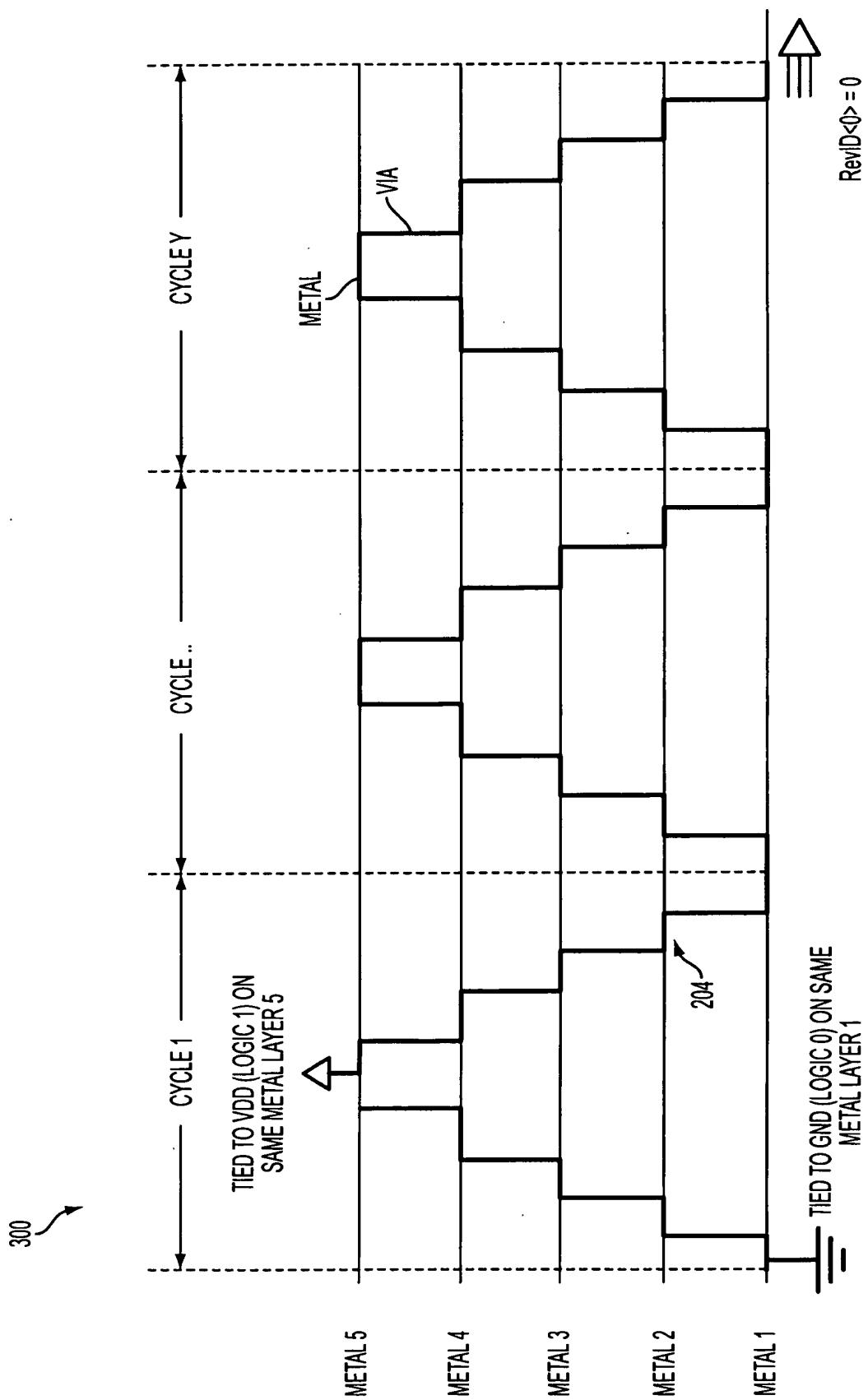


FIG. 3B

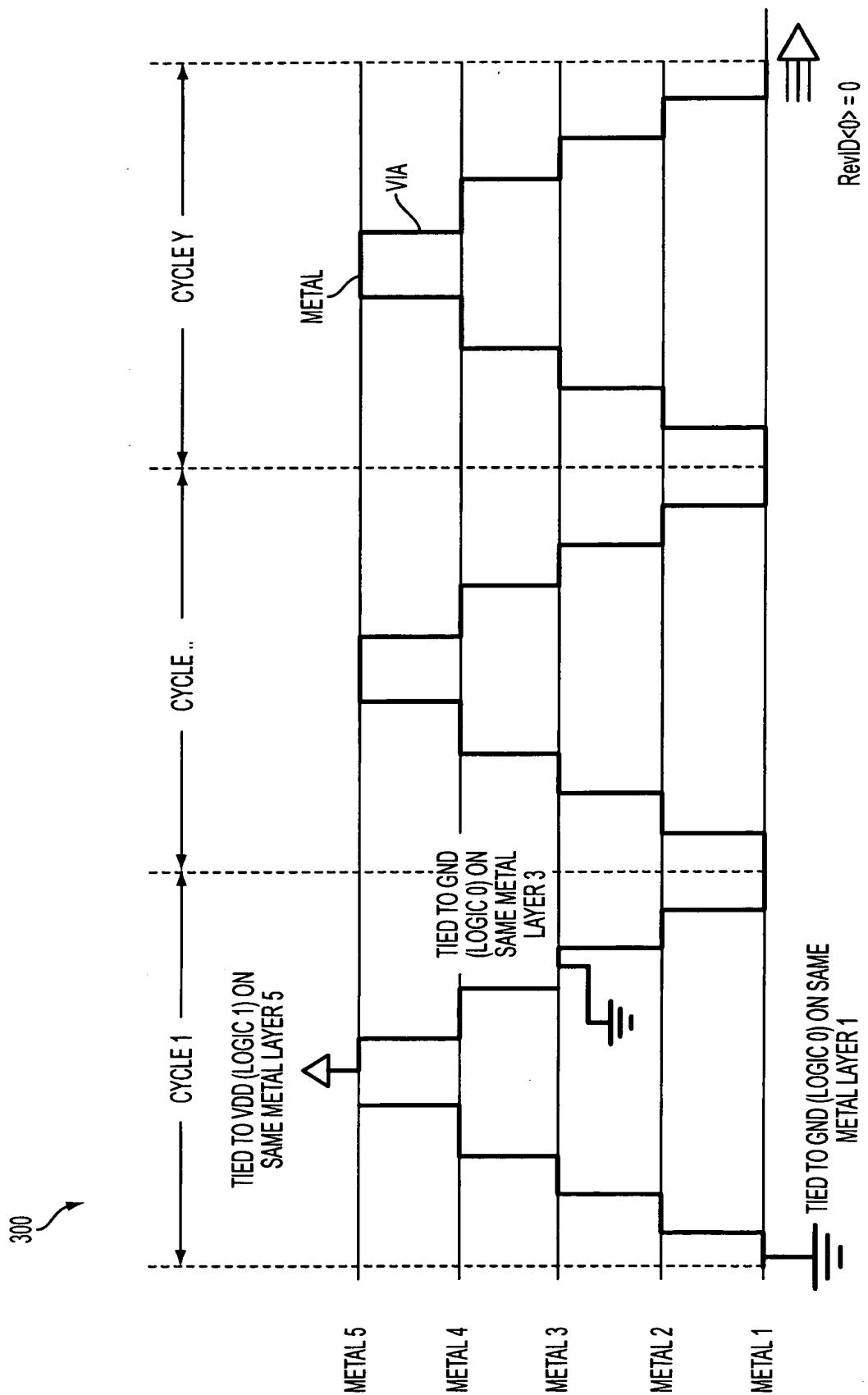


FIG. 3C

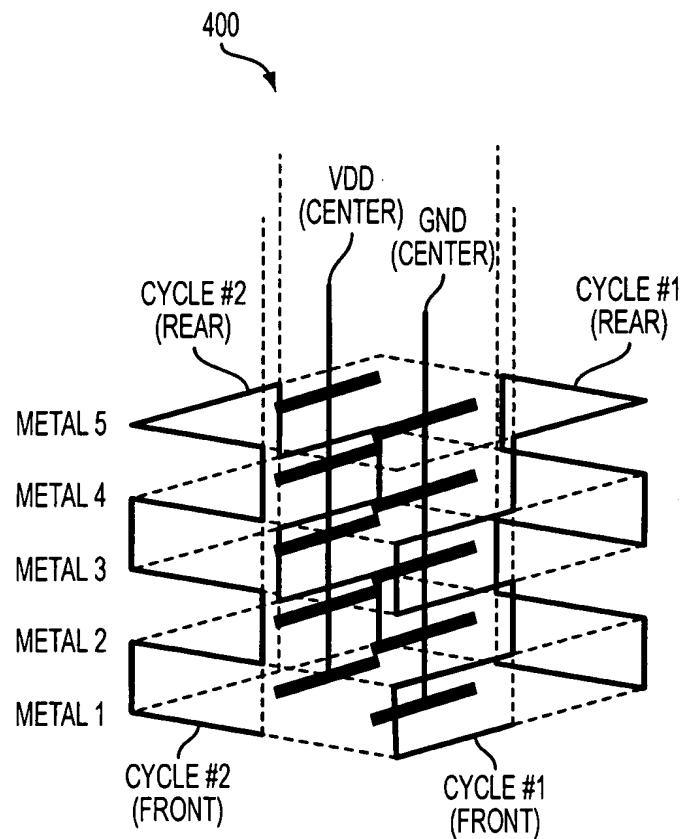


FIG. 4

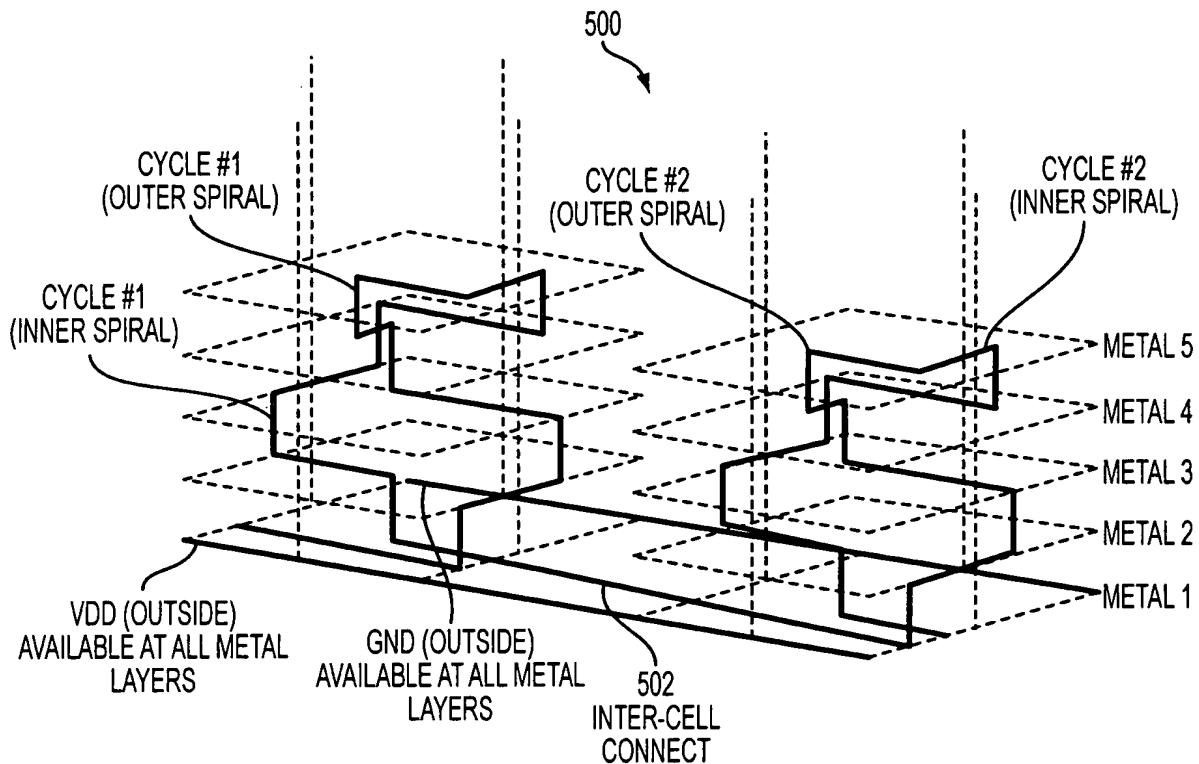


FIG. 5A

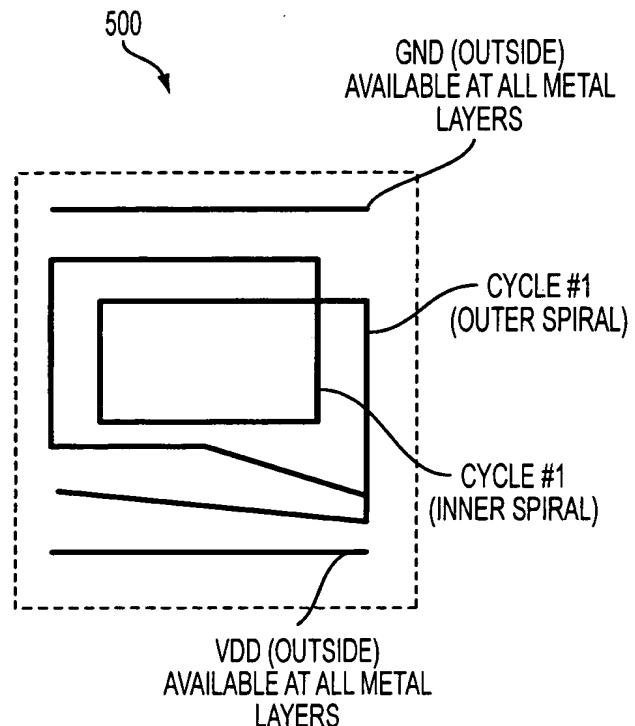


FIG. 5B

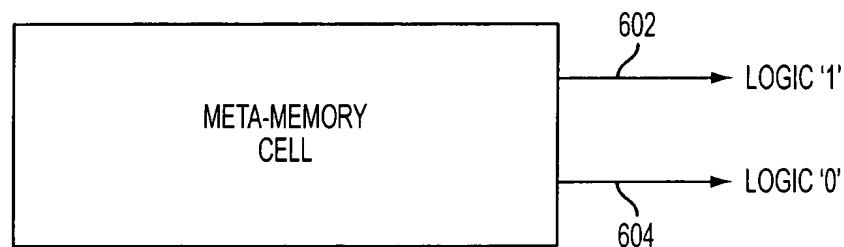


FIG. 6

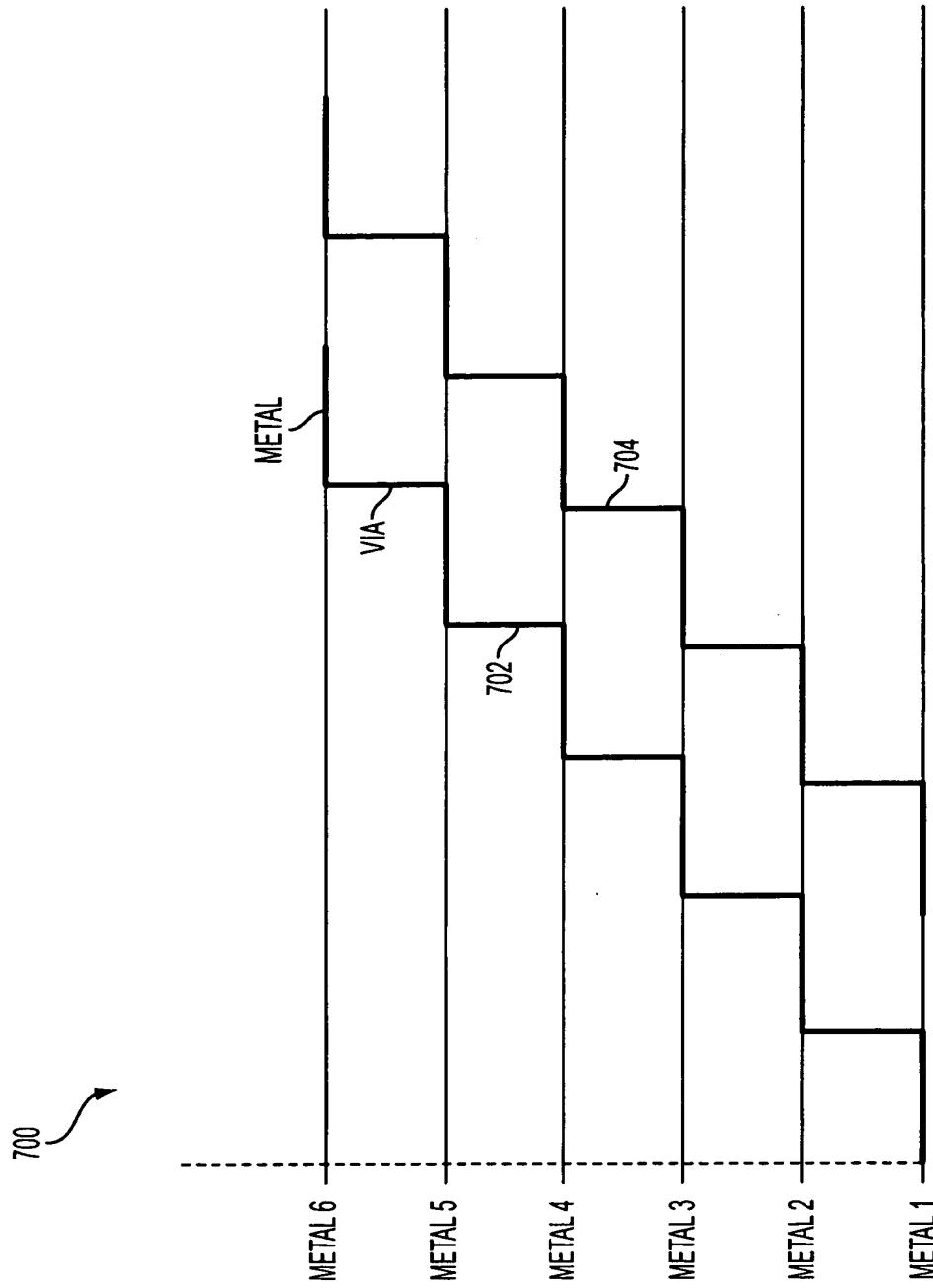


FIG. 7A

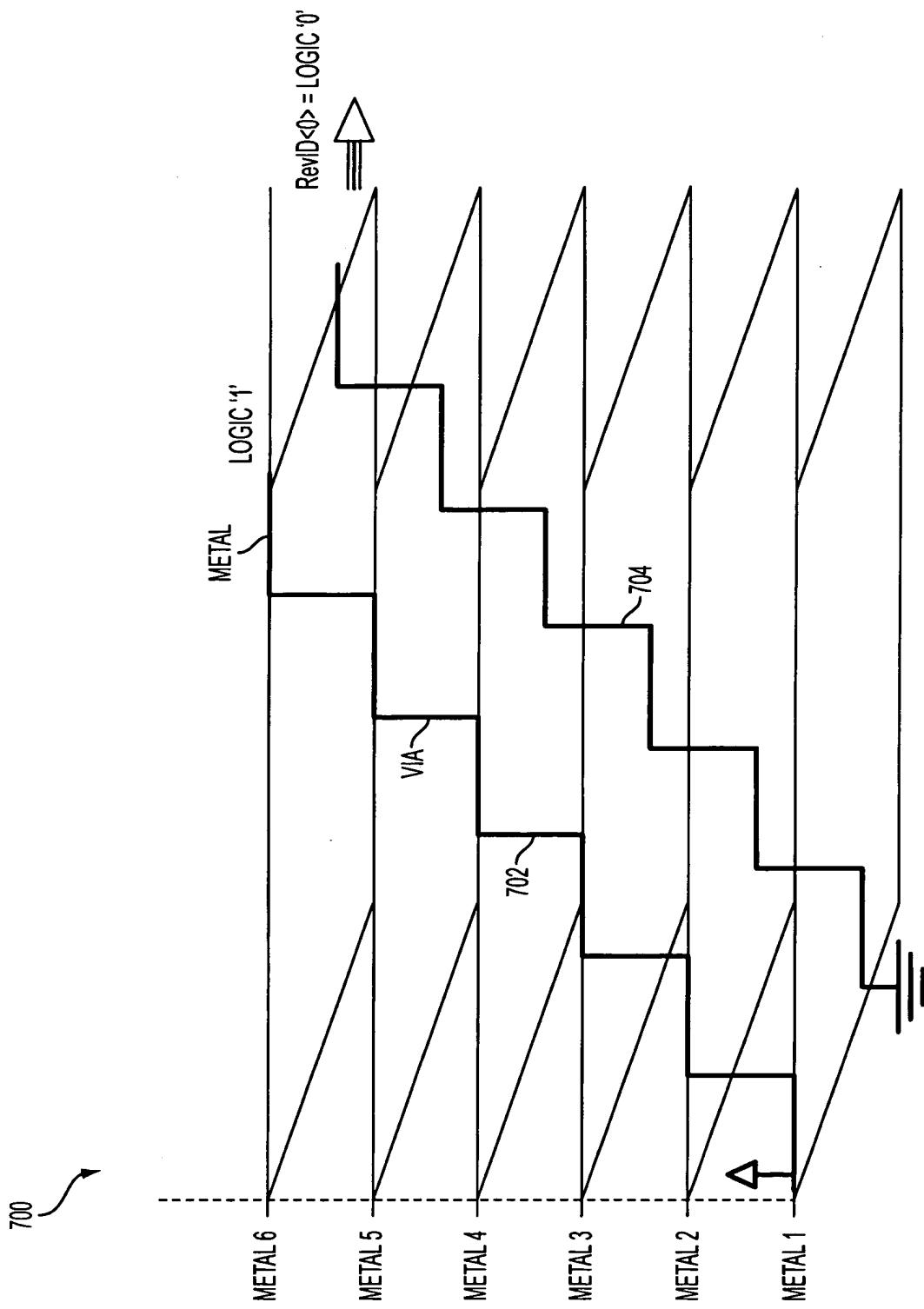


FIG. 7B

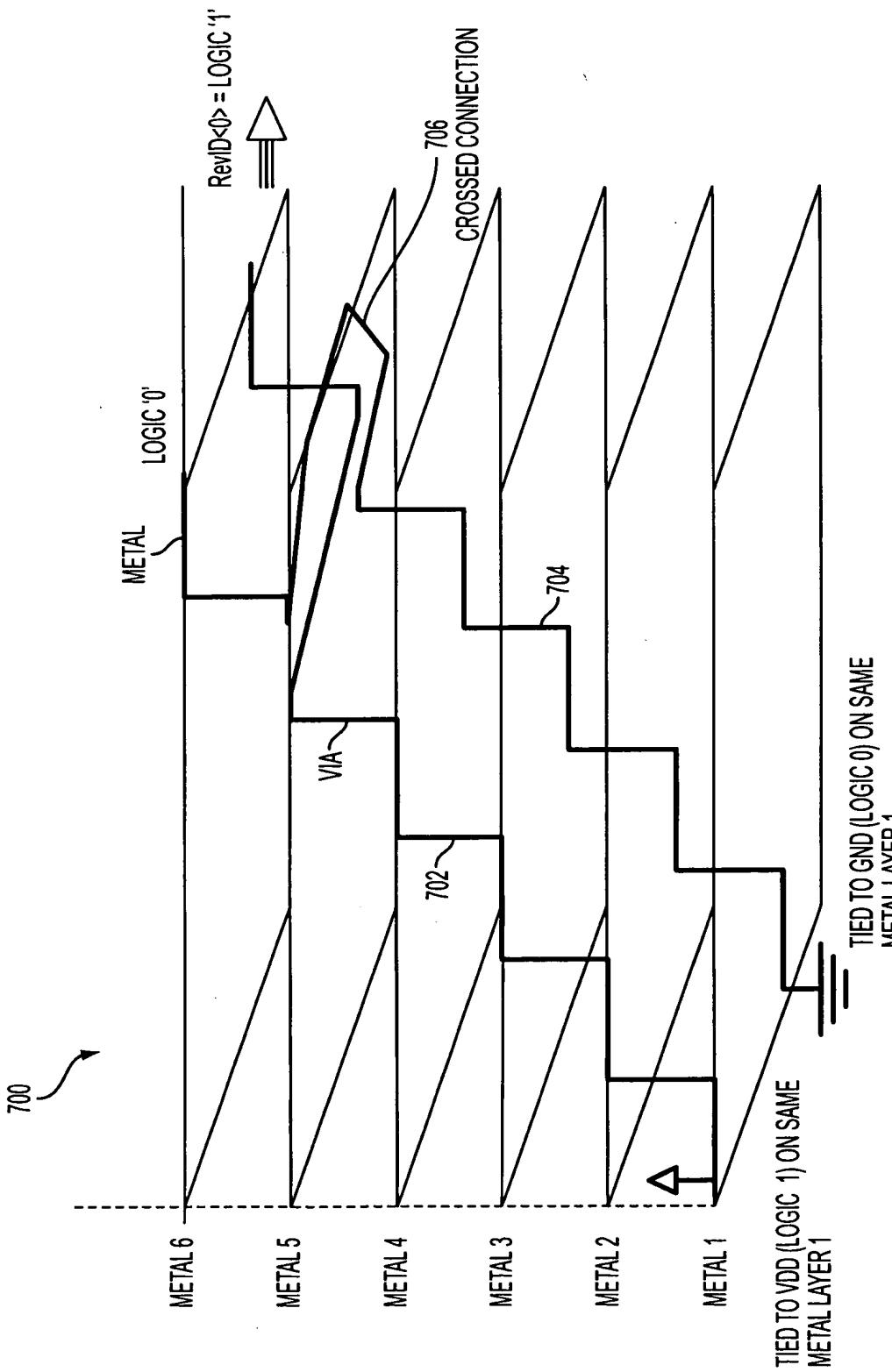


FIG. 7C

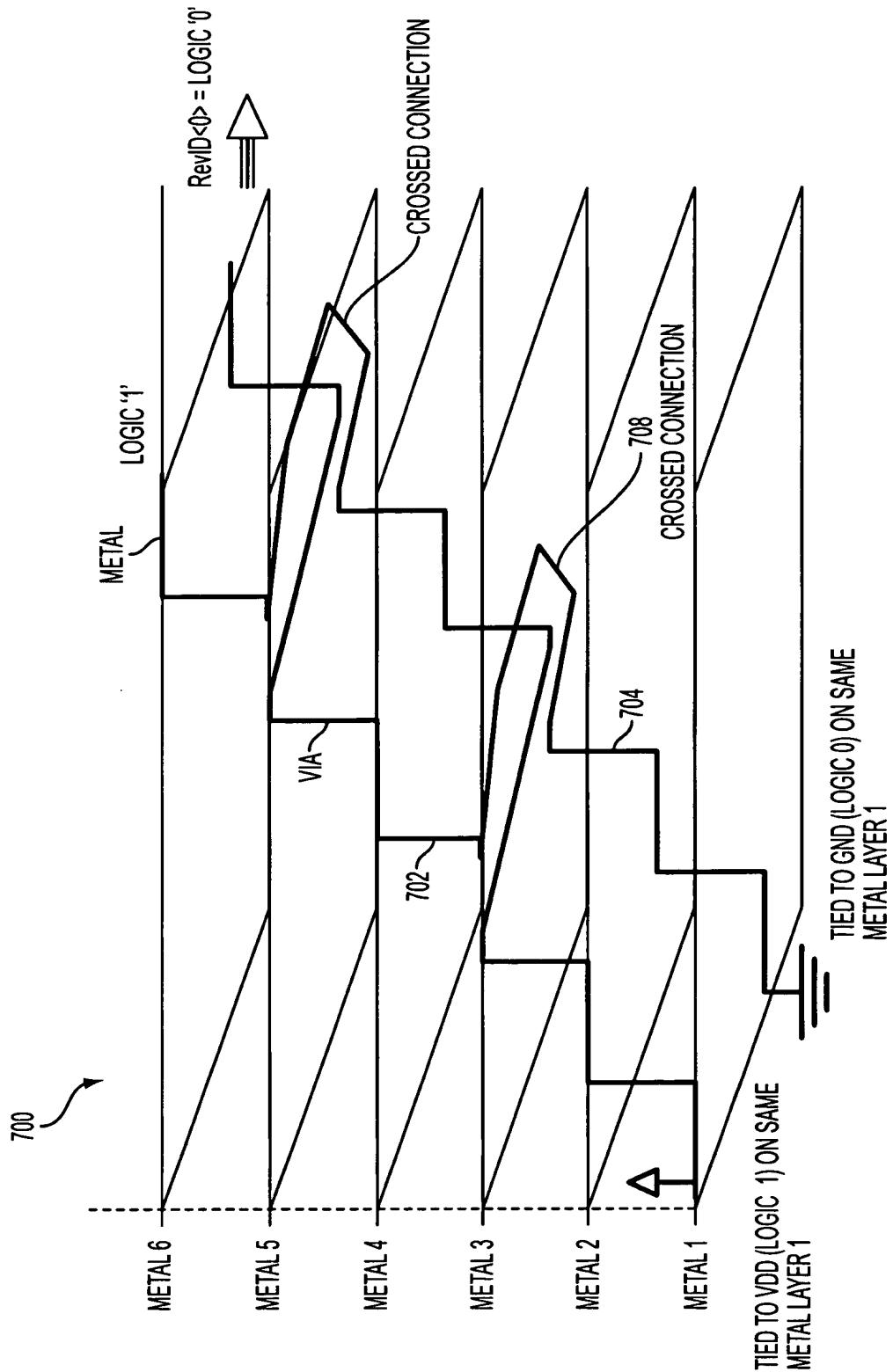


FIG. 7D

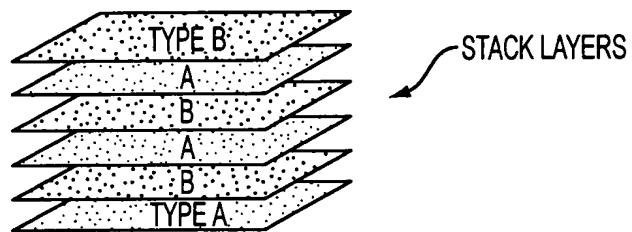


FIG. 8A

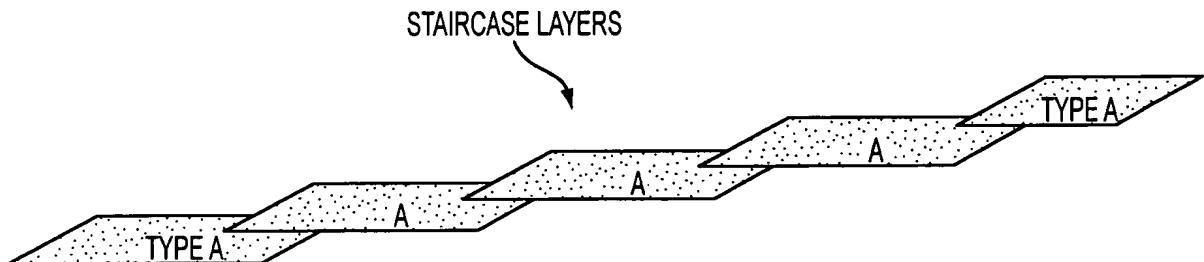


FIG. 8B

Replacement Sheet  
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Appl. No. 10/697,289; Filed: Oct 31, 2003  
Dkt No. 1875.4360005; Group Unit: 2819  
Inventors: CATALASAN et al.  
Tel. No.: 202-371-2600  
For: Coupling of Signals Between Adjacent Functional  
Blocks in an Integrated Circuit Chip

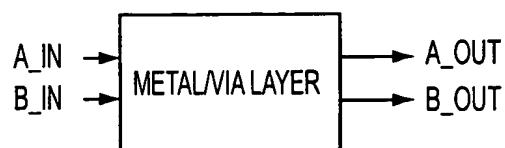


FIG. 9A

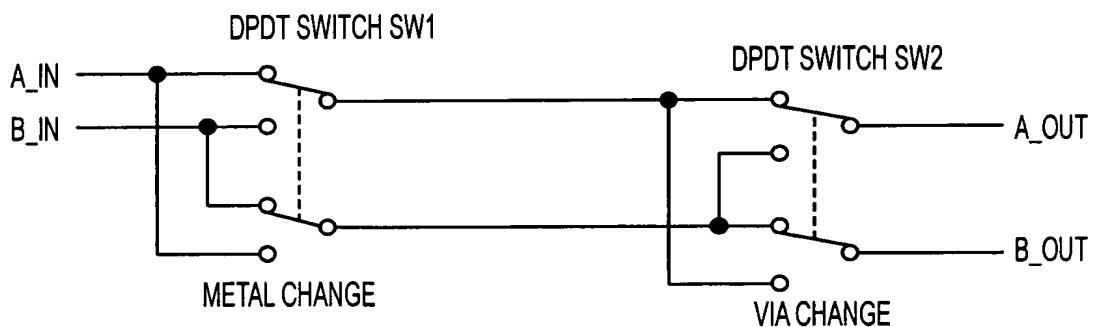


FIG. 9B

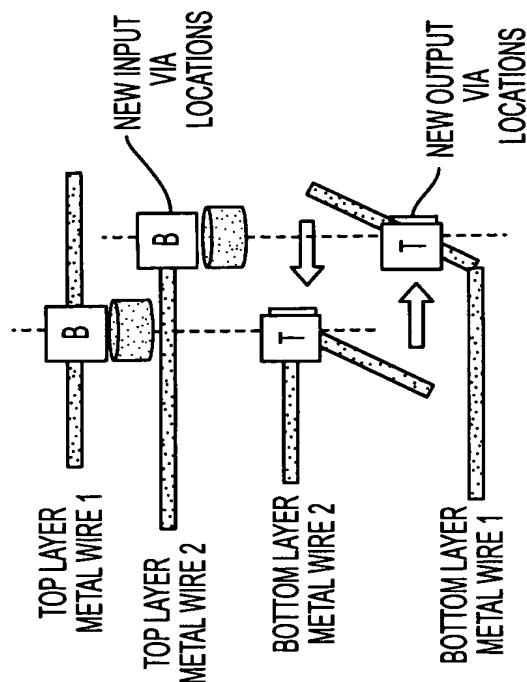


FIG. 9D

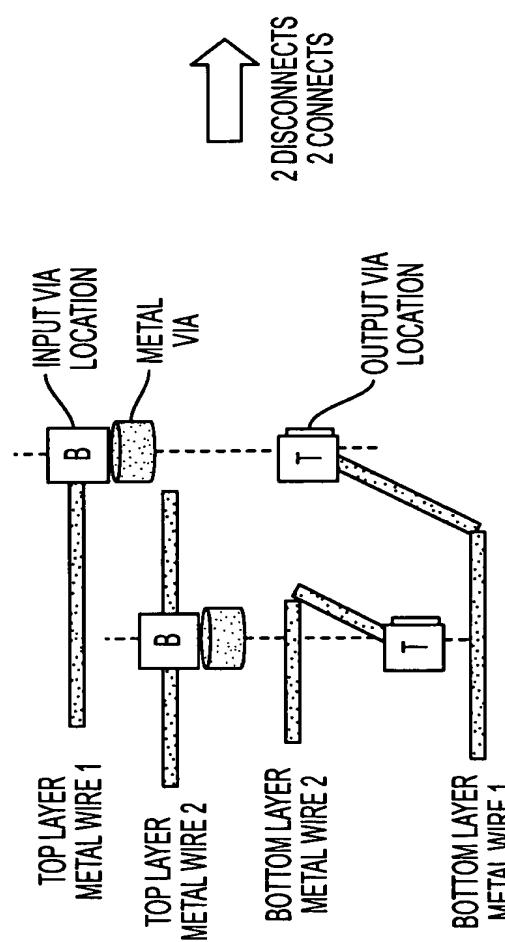


FIG. 9C

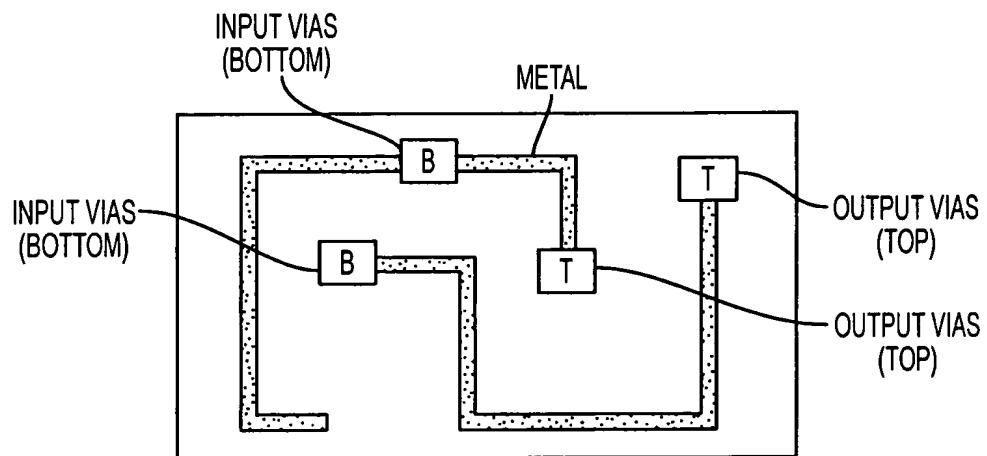


FIG. 10A

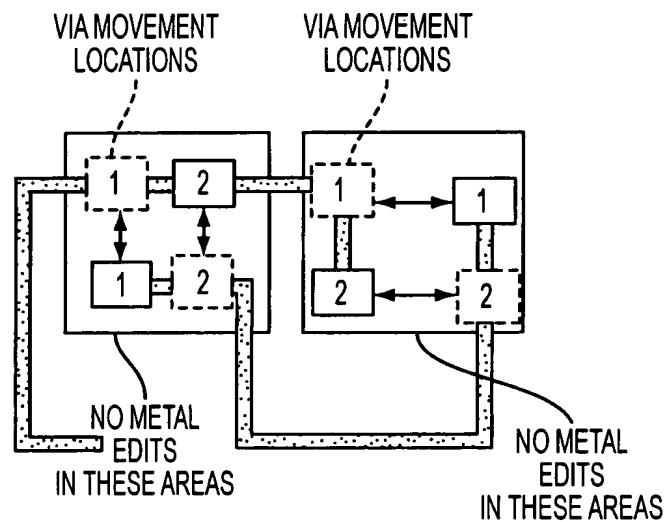
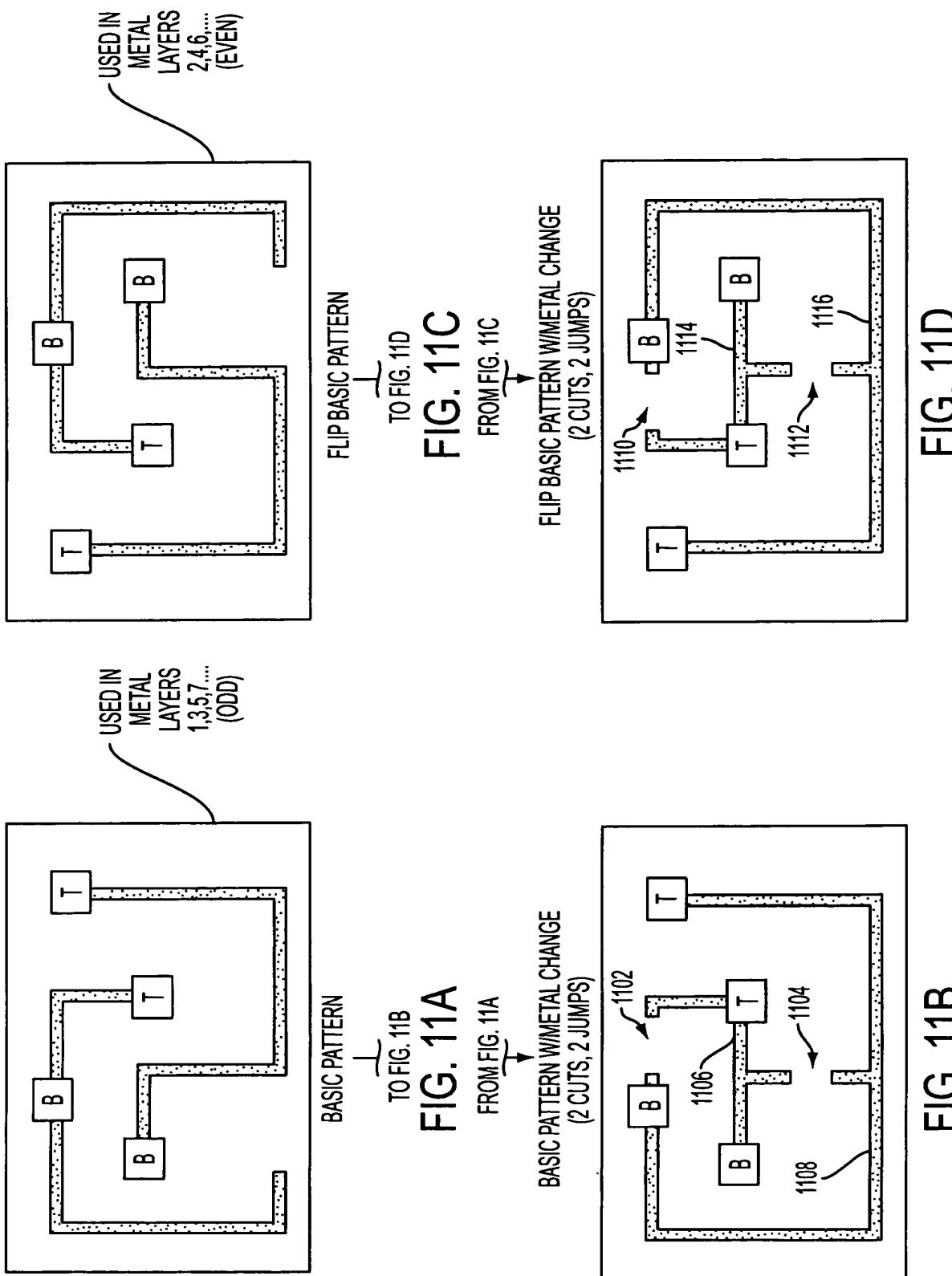
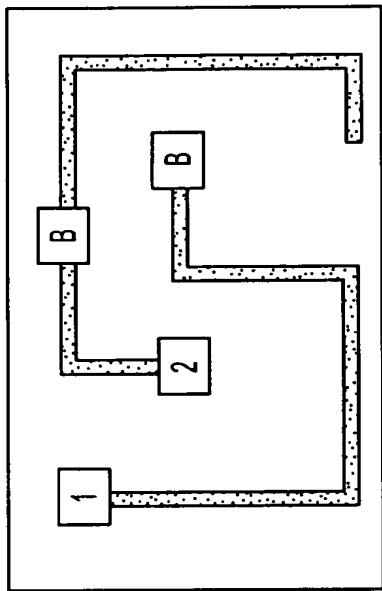


FIG. 10B





FROM FIG. 12A

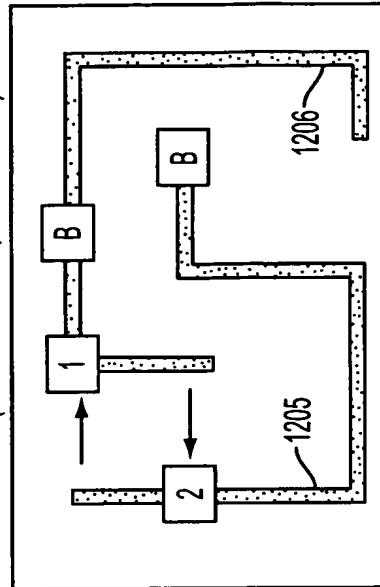


TO FIG. 12B

FIG. 12A

FROM FIG. 12C

FLIP BASIC PATTERN VIA CHANGE  
(2 DISCONNECTS, 2 CONNECTS)



TO FIG. 12D

FIG. 12C

FIG. 12D

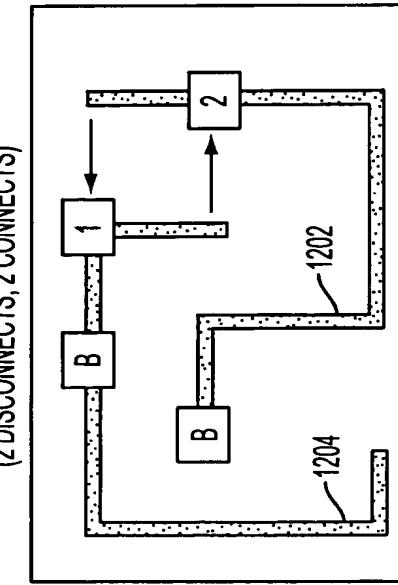
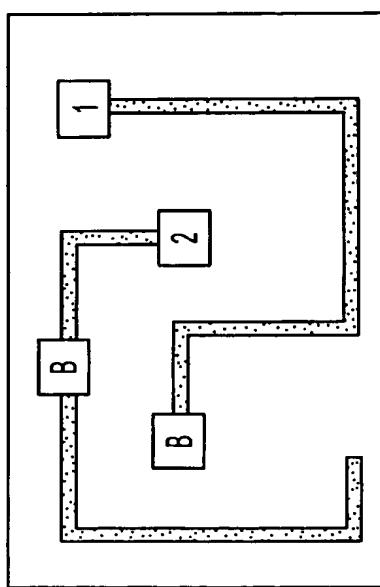


FIG. 12B

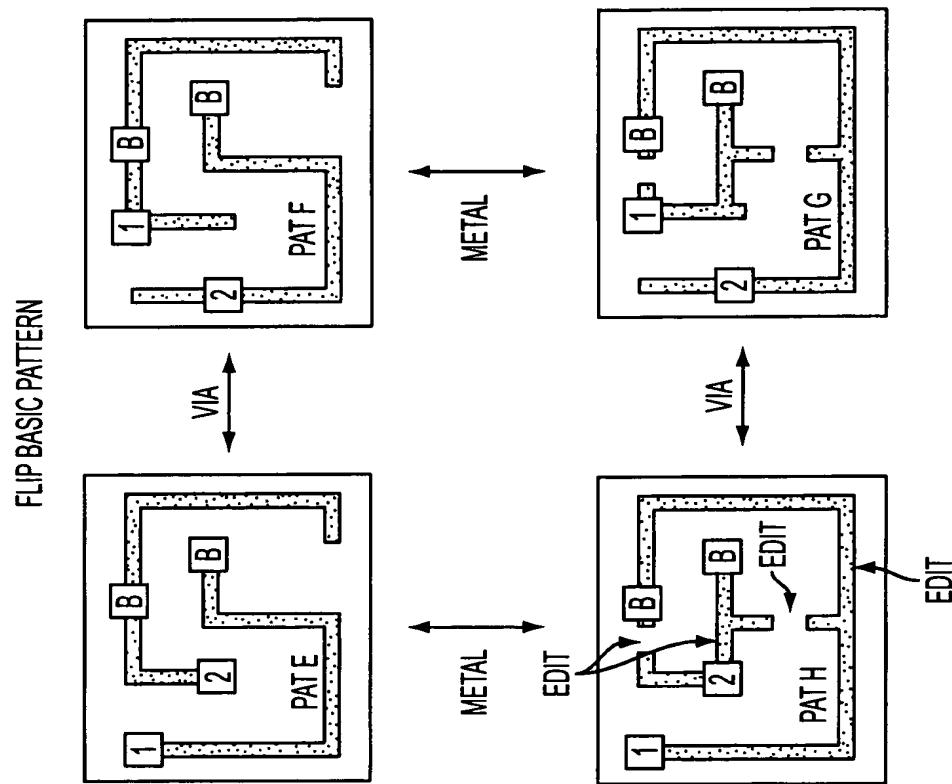


FIG. 14

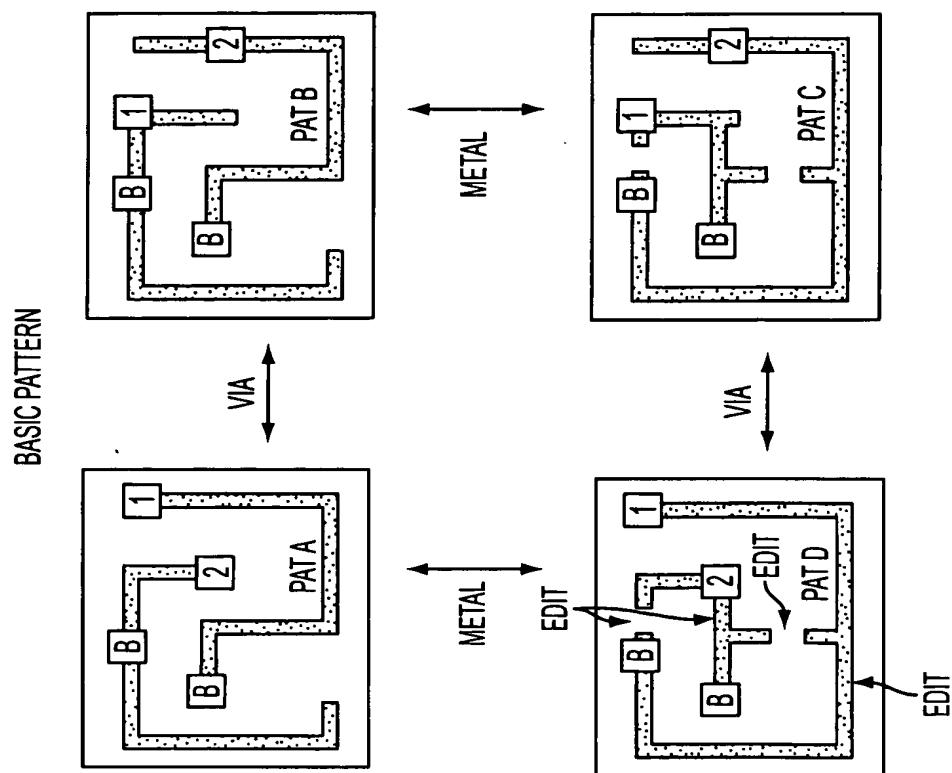
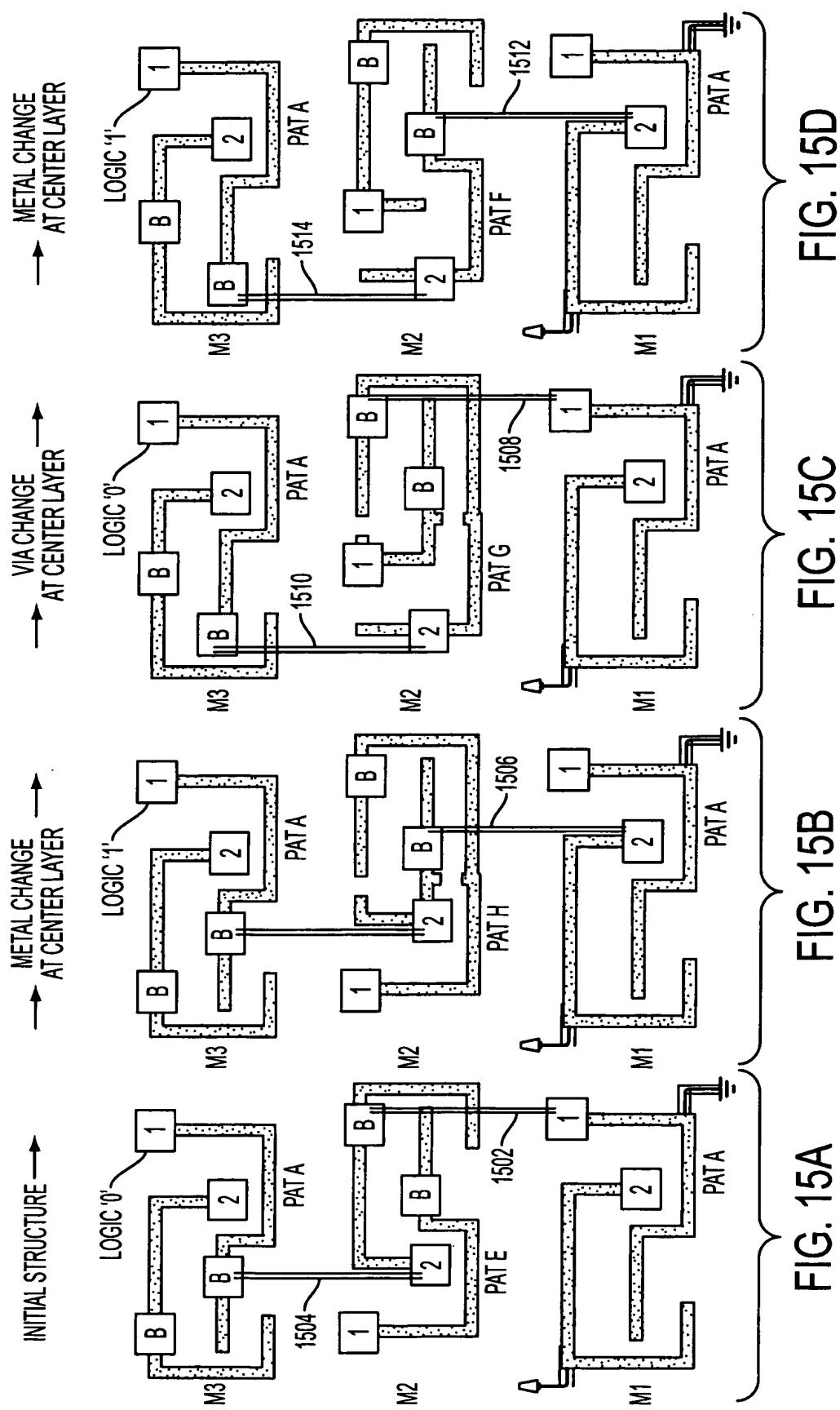


FIG. 13



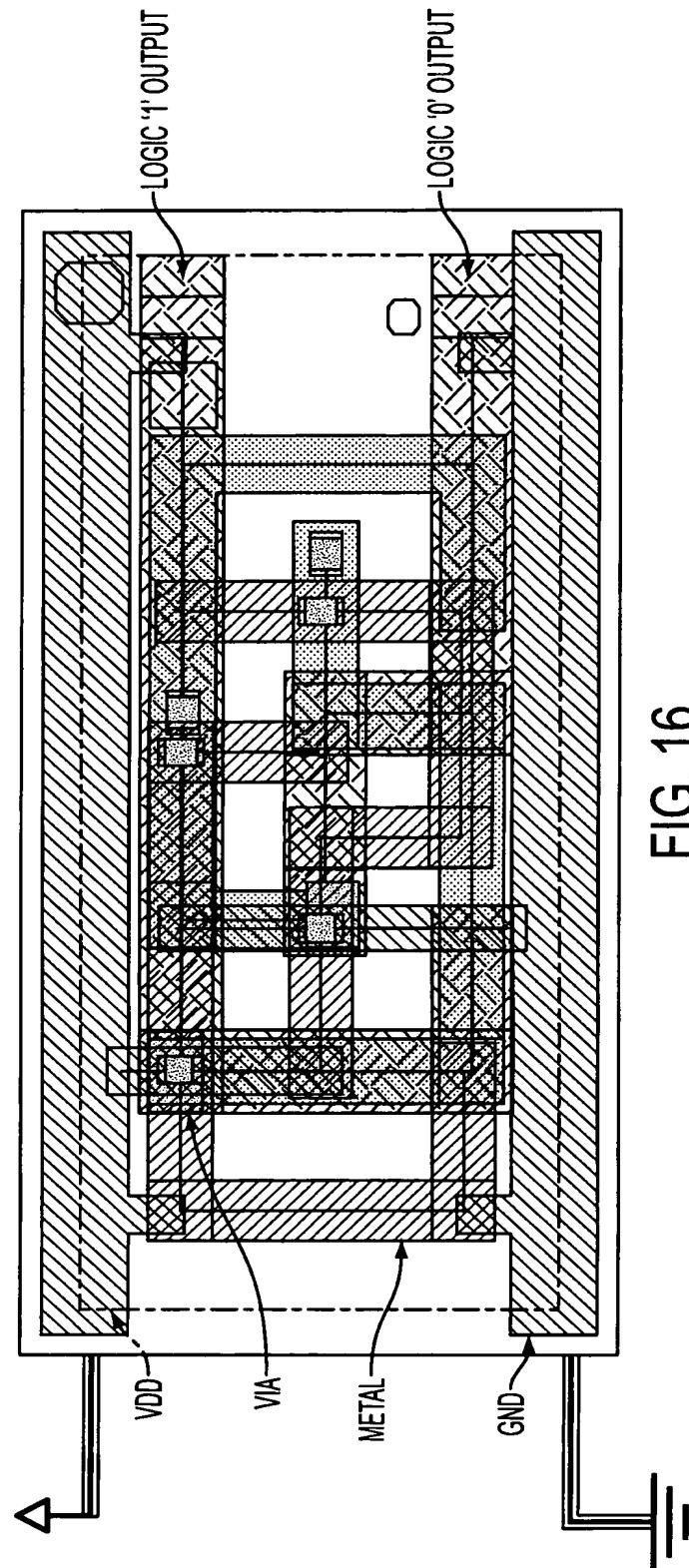
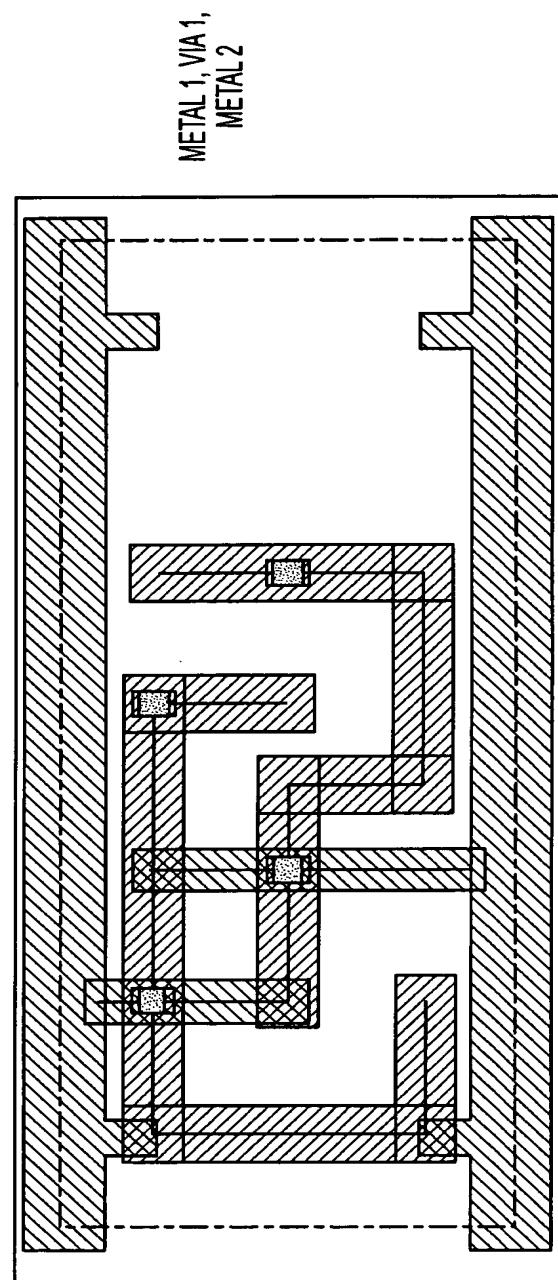
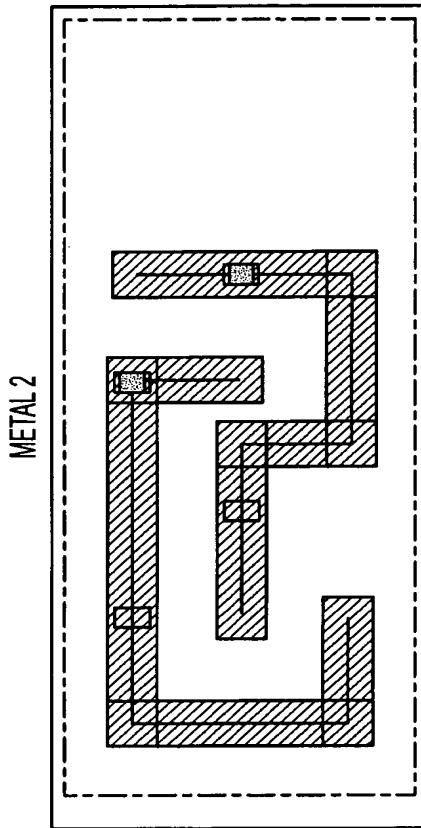
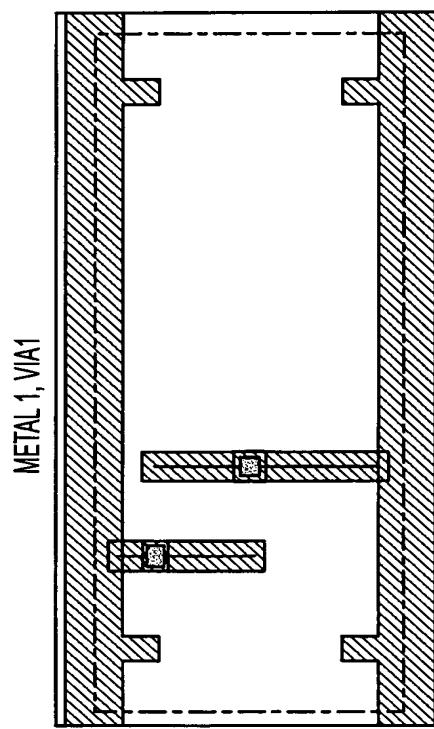


FIG. 16



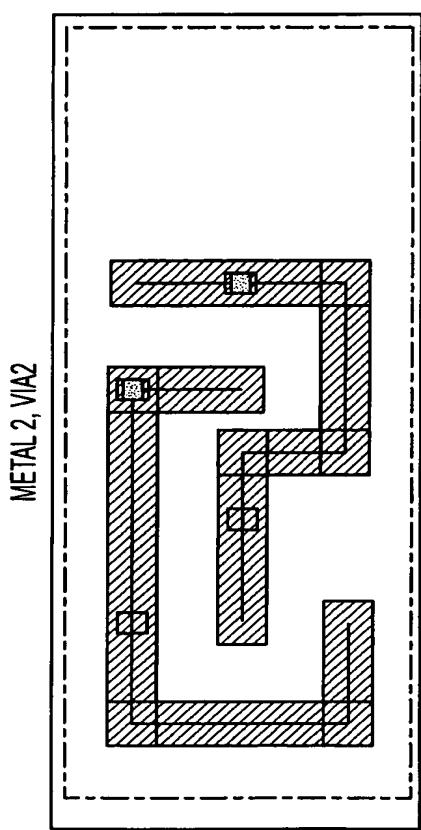


FIG. 18A

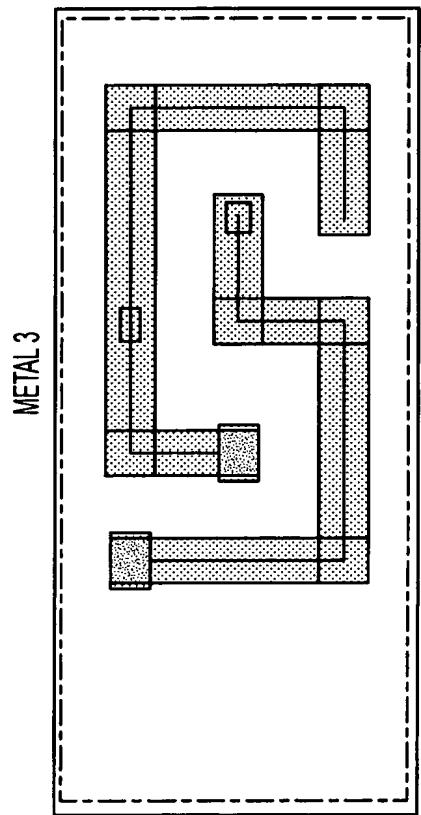


FIG. 18B

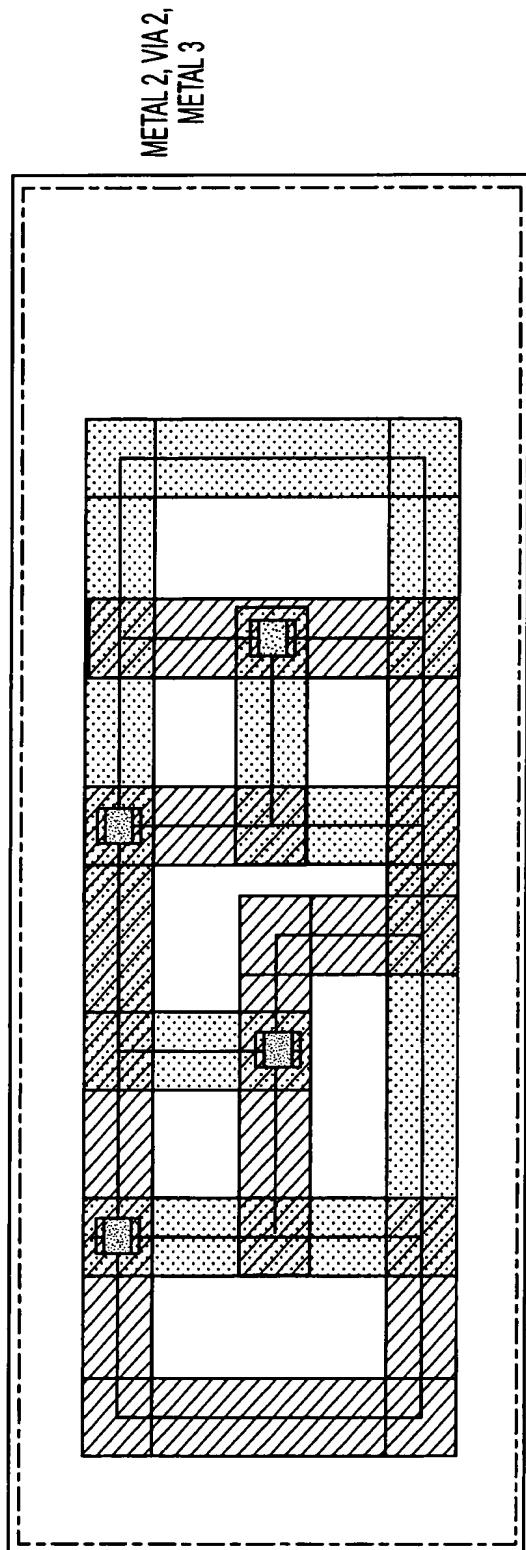


FIG. 18C

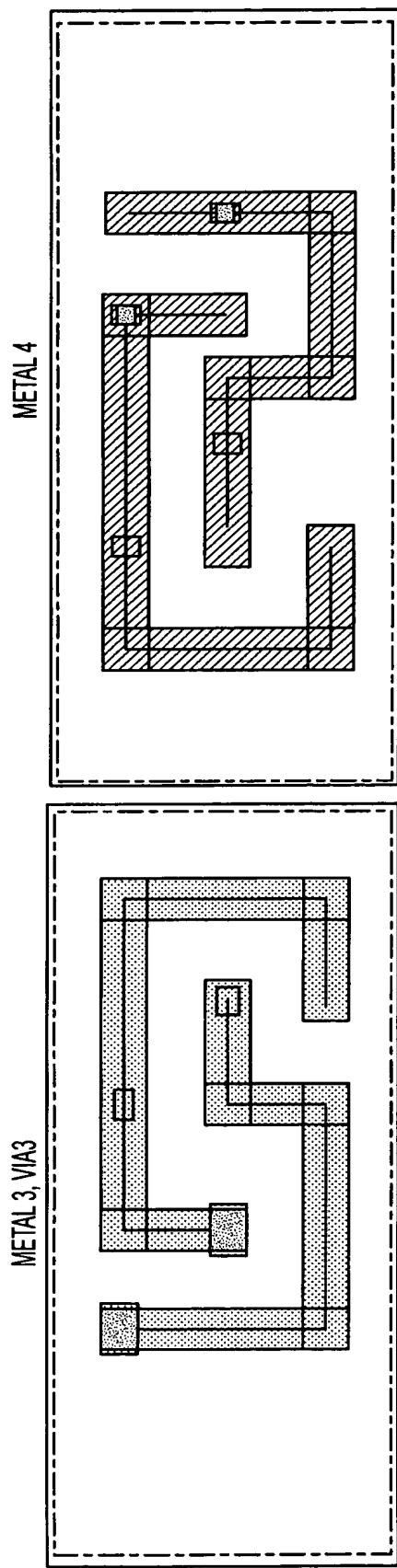


FIG. 19B

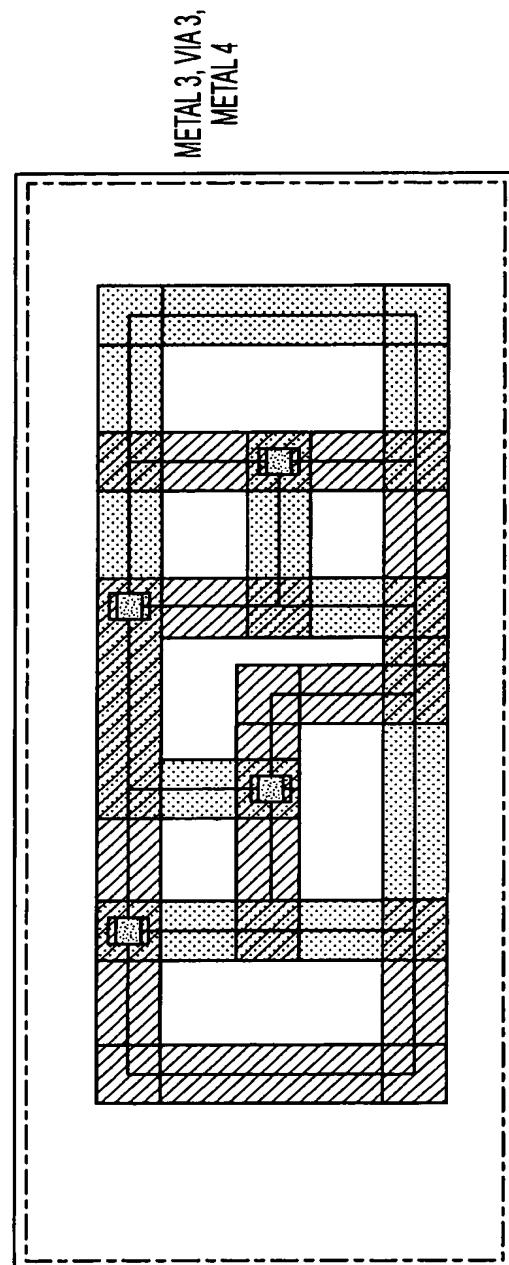


FIG. 19C

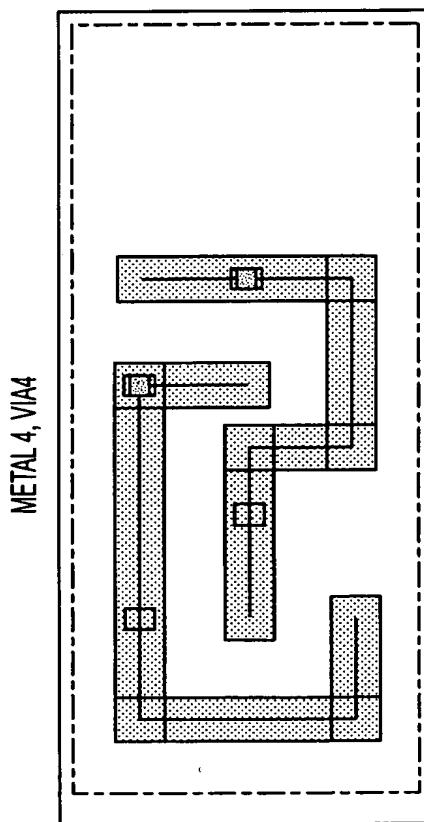
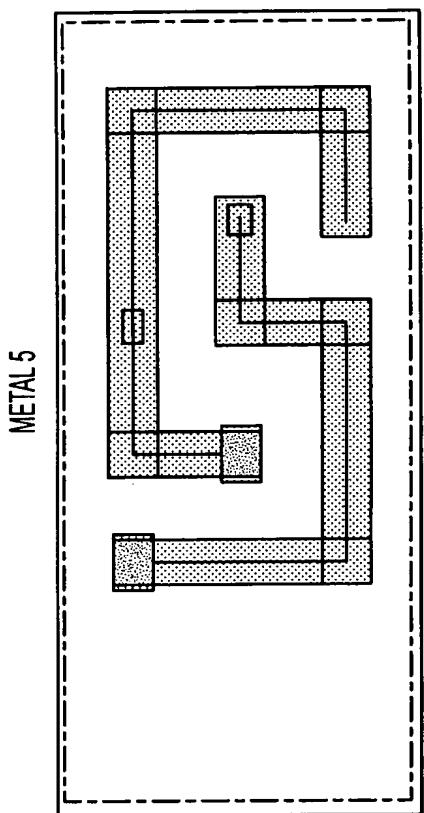


FIG. 20A  
FIG. 20B

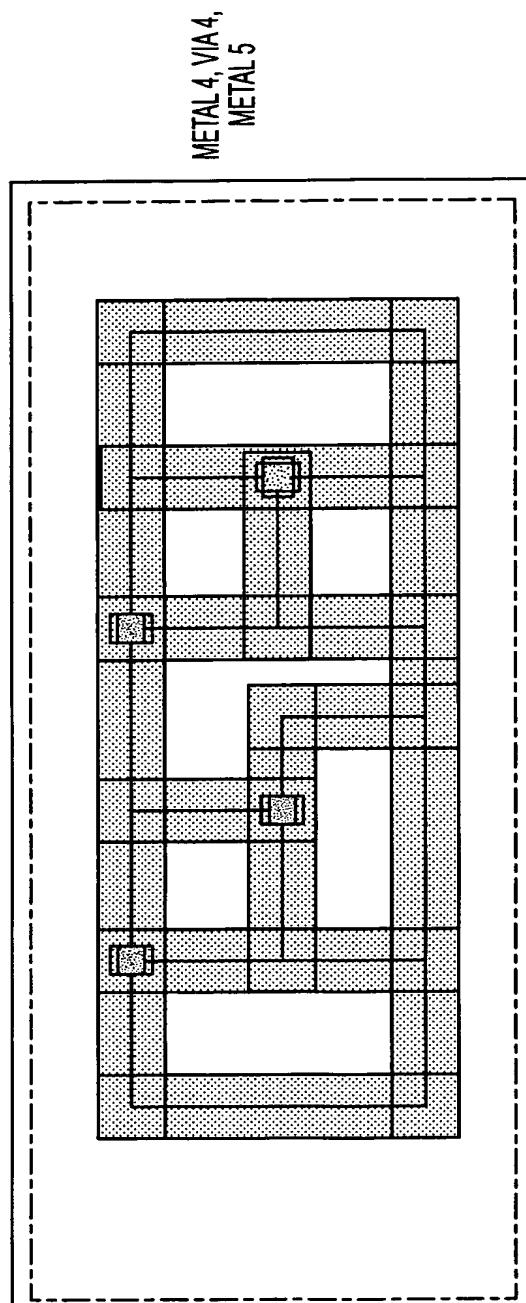


FIG. 20C

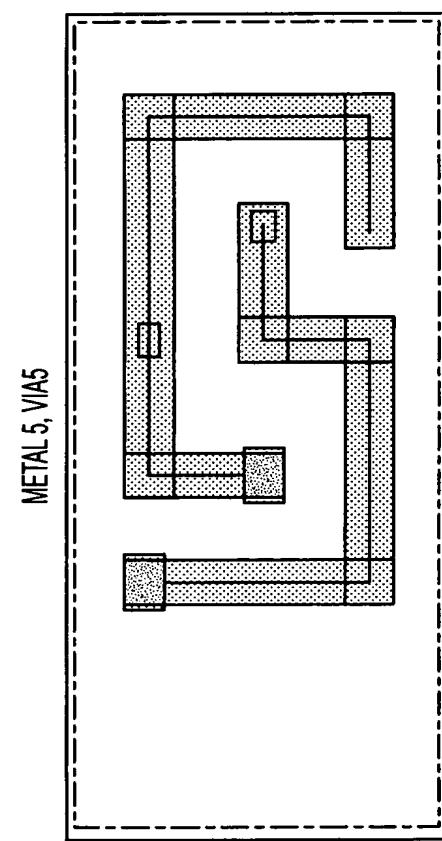


FIG. 21A

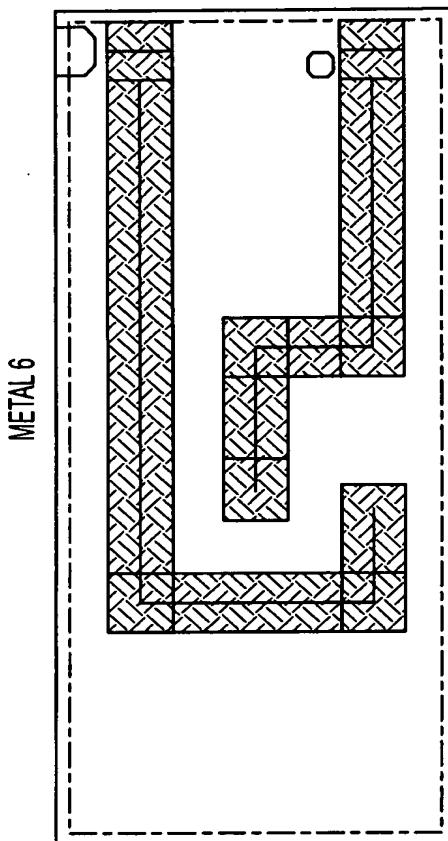


FIG. 21B

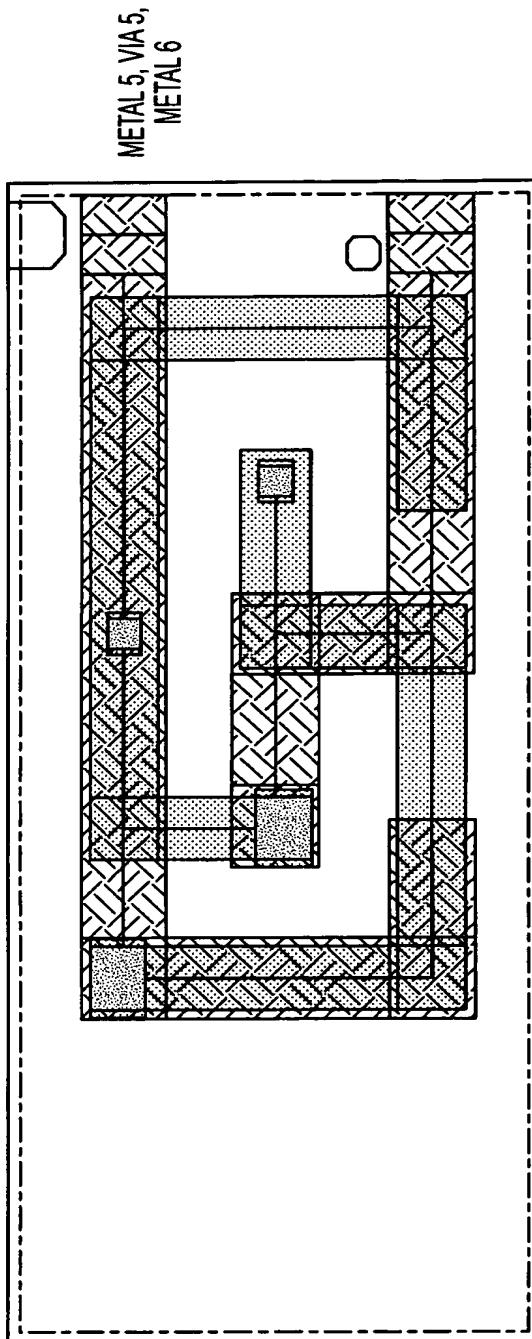


FIG. 21C

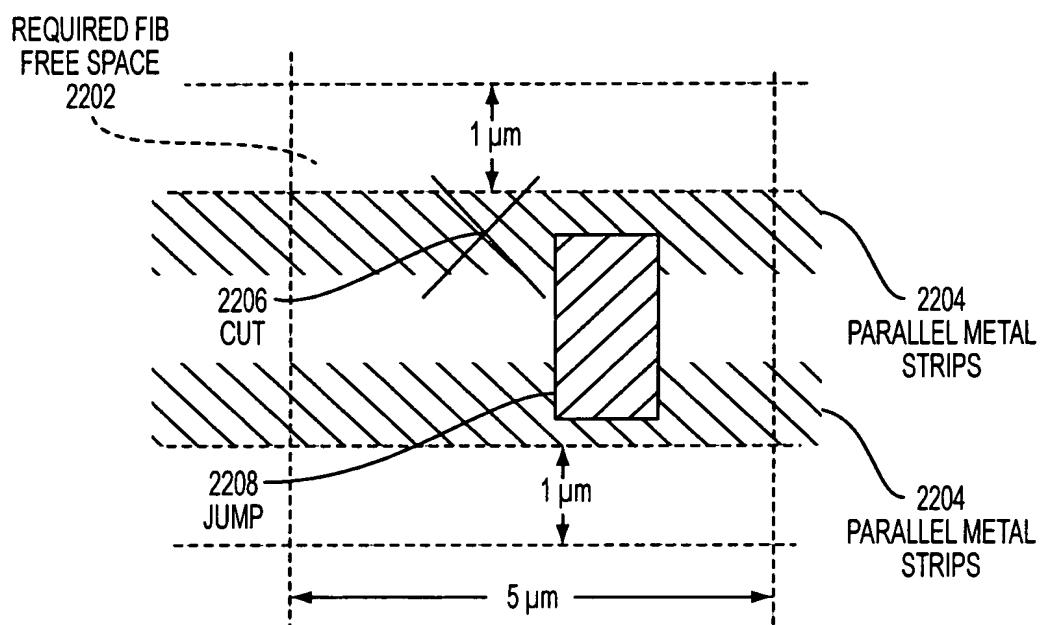


FIG. 22

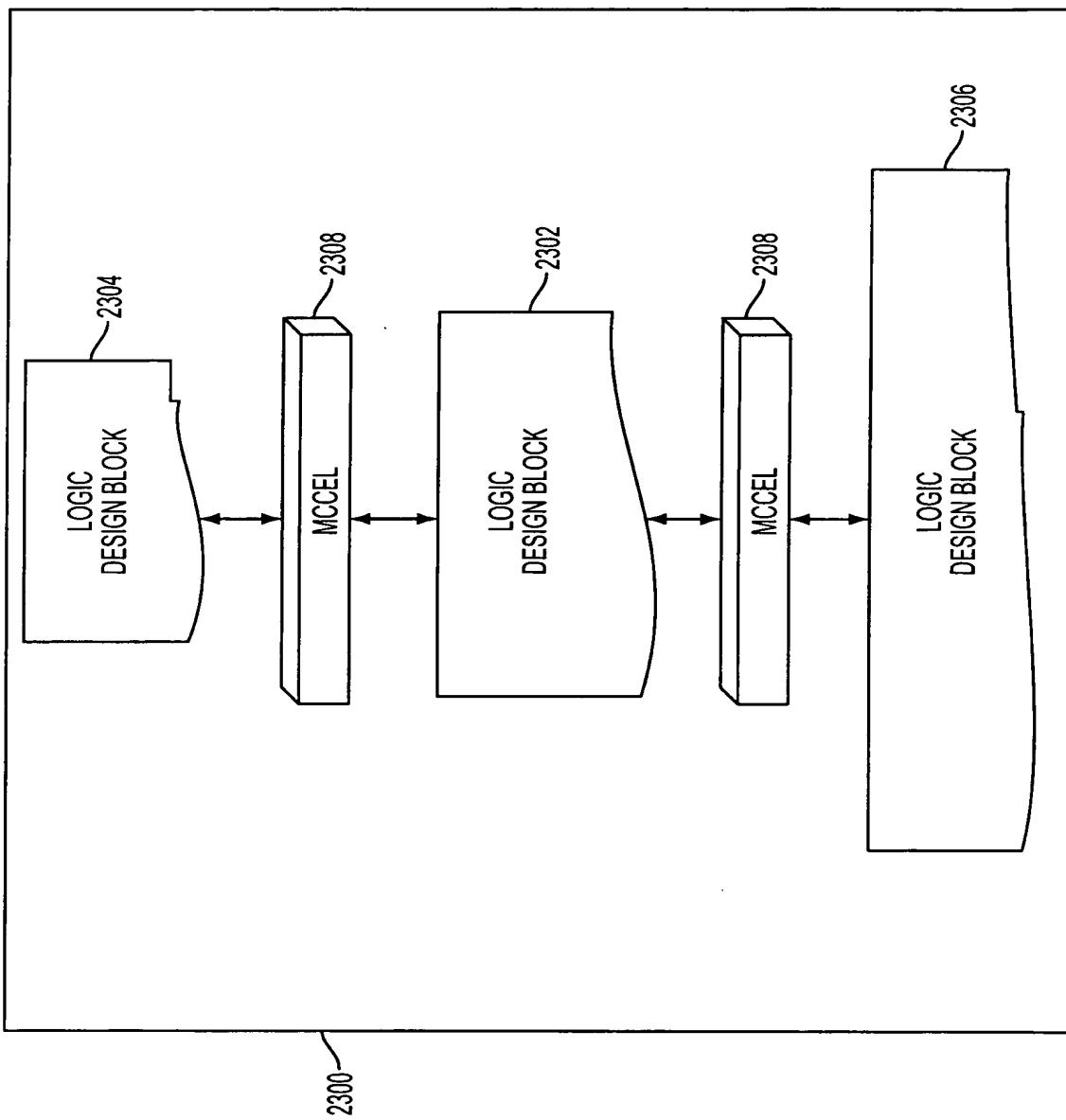


FIG. 23

Replacement Sheet  
Sheet 29 of 42  
Appl. No. 10/697,289; Filed: Oct 31, 2003  
Dkt No. 1875.4360005; Group Unit: 2819  
Inventors: CATALASAN et al.  
Tel. No.: 202-371-2600  
For: Coupling of Signals Between Adjacent Functional  
Blocks in an Integrated Circuit Chip

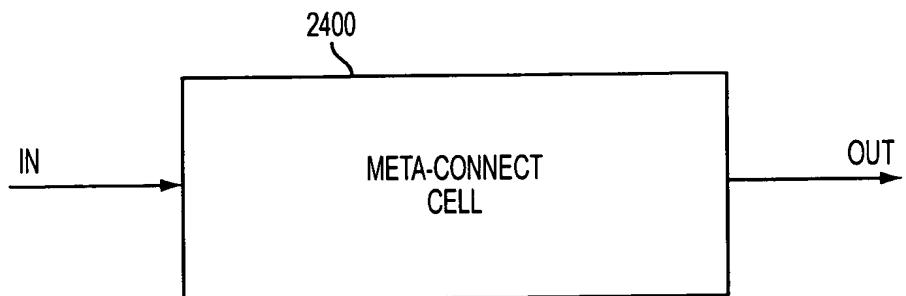


FIG. 24A

OUT	COMMENT
IN	DEFAULT CONNECT AT ANY LAYER
0	TIED TO GND AT ANY LAYER
1	TIED TO VDD AT ANY LAYER

FIG. 24B

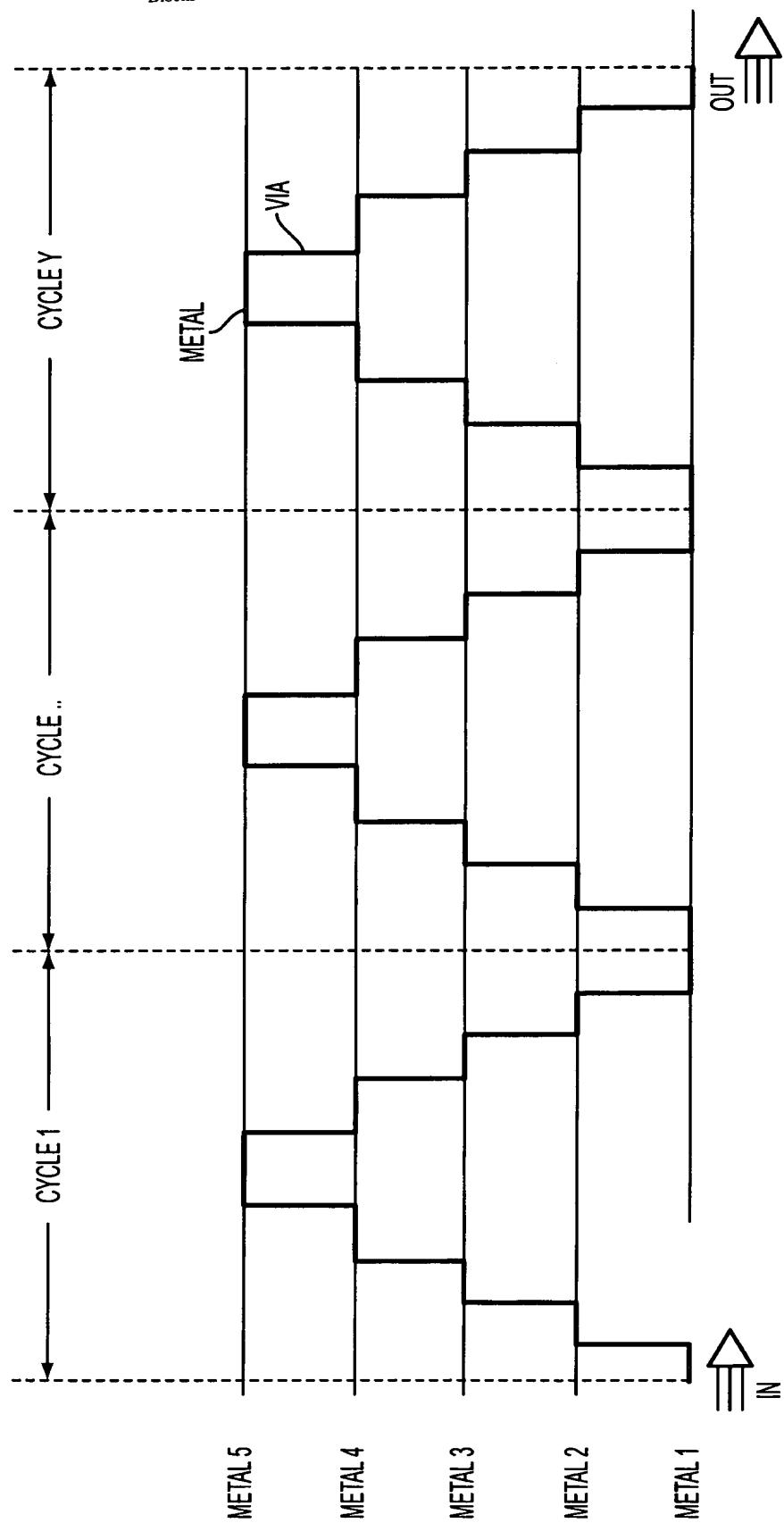


FIG. 25

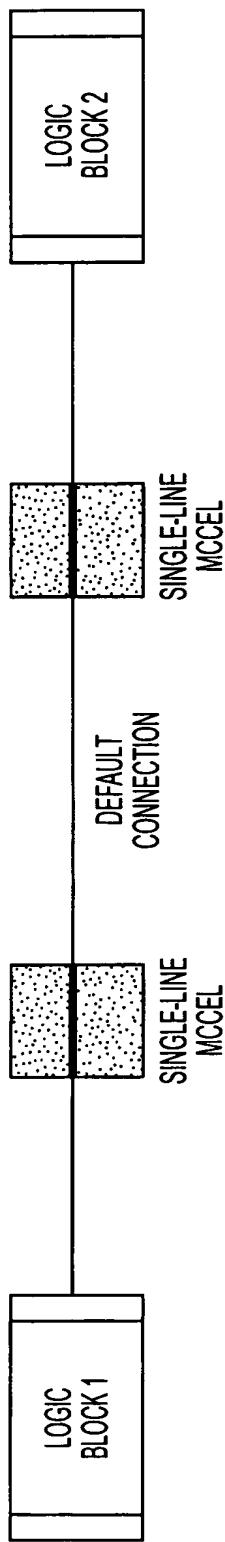


FIG. 26A

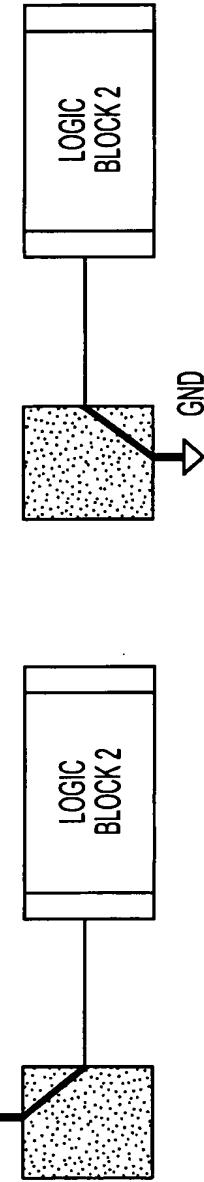


FIG. 26B

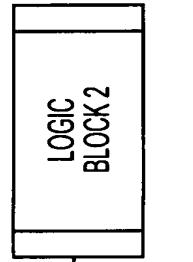


FIG. 26C

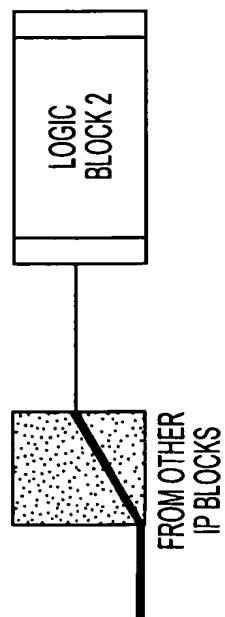


FIG. 26D

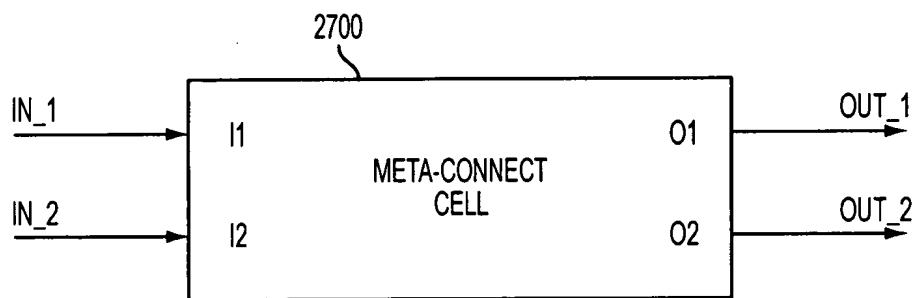


FIG. 27A

TOGGLE	OUT_1	OUT_2	COMMENT
0	IN_1	IN_2	DEFAULT
1	IN_2	IN_1	METAL/VIA CHANGE

FIG. 27B

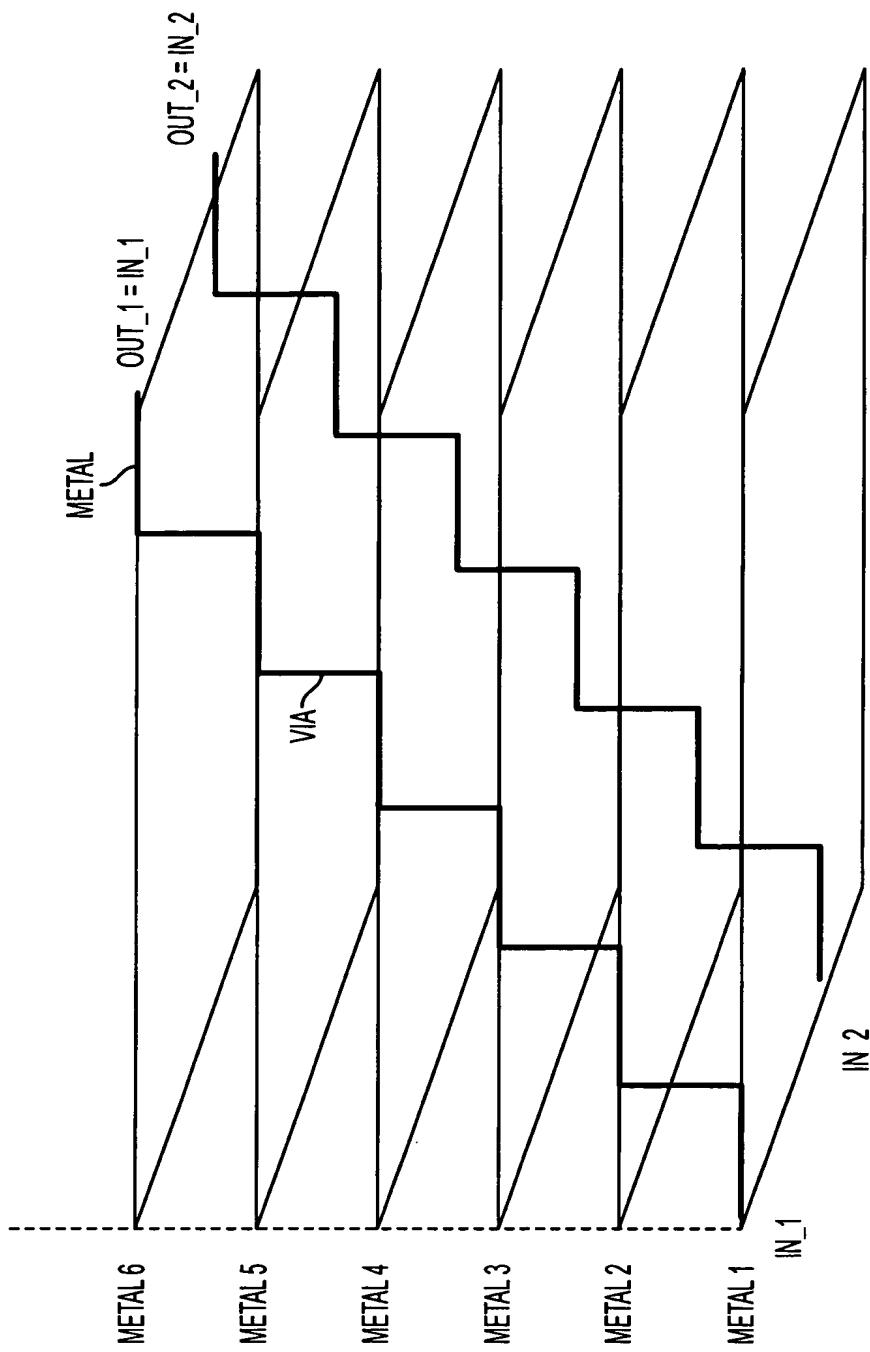


FIG. 28

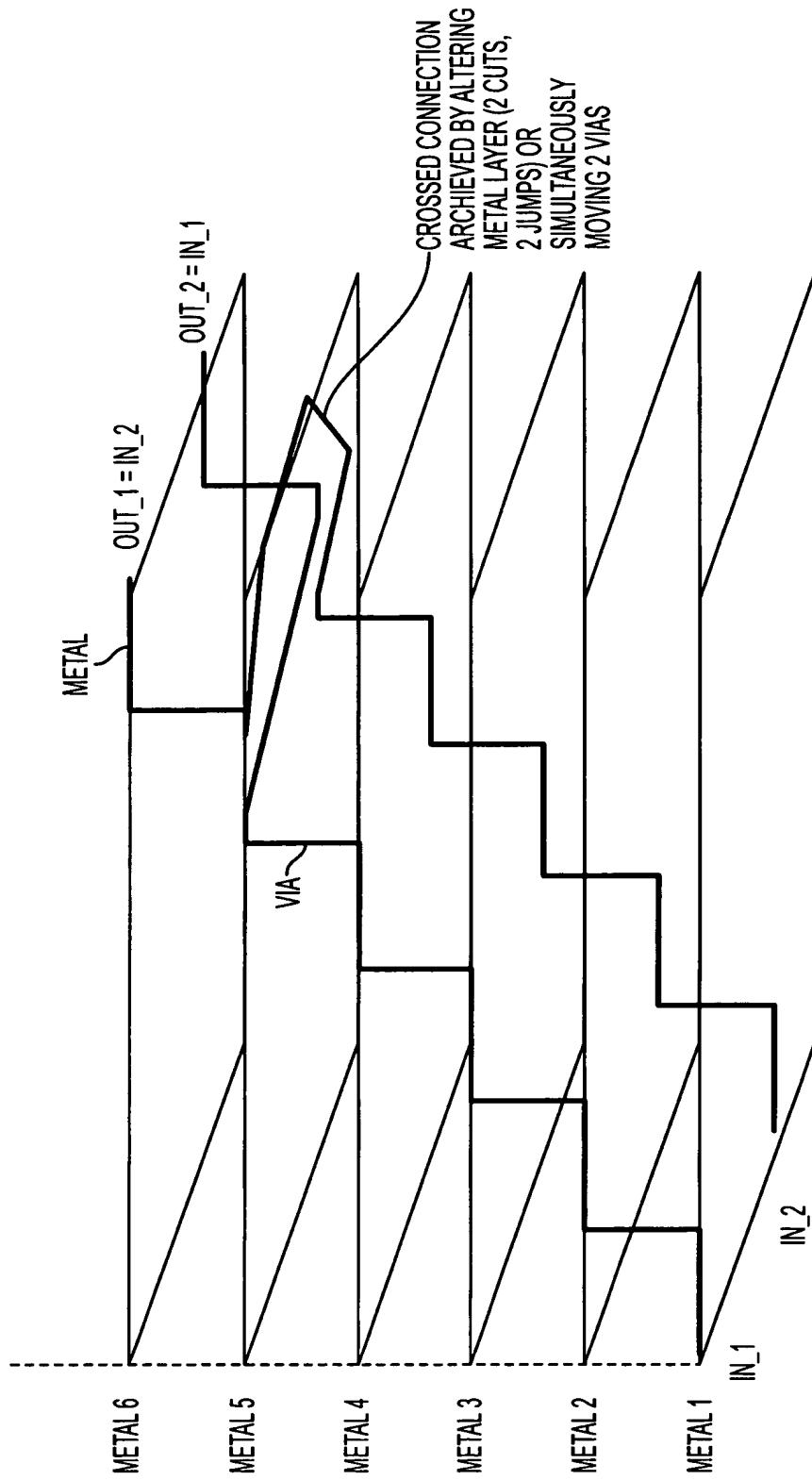


FIG. 29

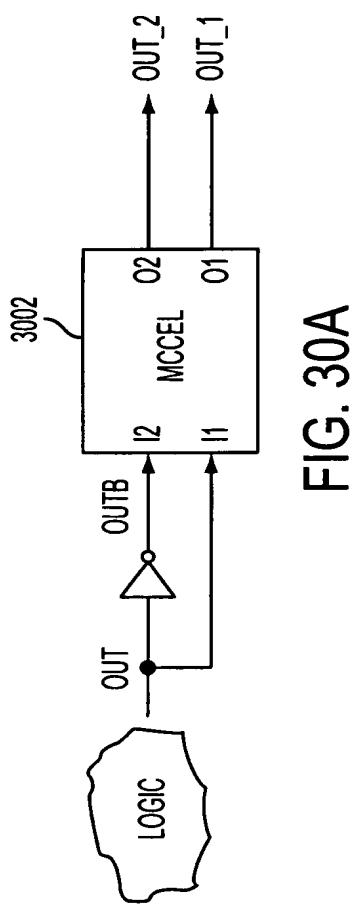


FIG. 30A

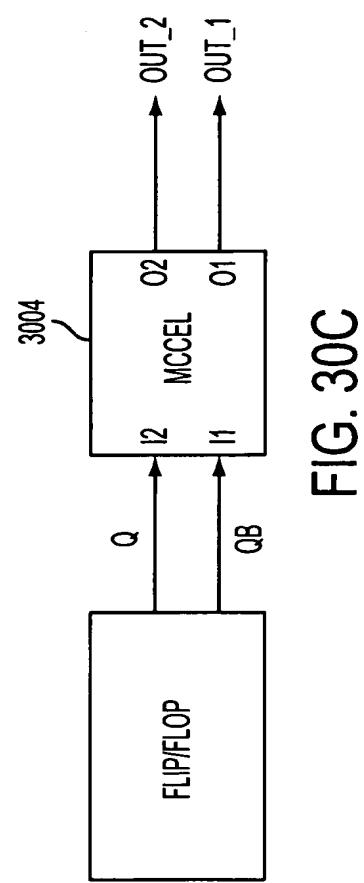


FIG. 30D

OUT_1	OUT_2	COMMENT
OUT	OUT	DEFAULT
OUTB	OUT	METAL/VIA CHANGE

FIG. 30B

OUT_1	OUT_2	COMMENT
Q	QB	DEFAULT
QB	Q	METAL/VIA CHANGE

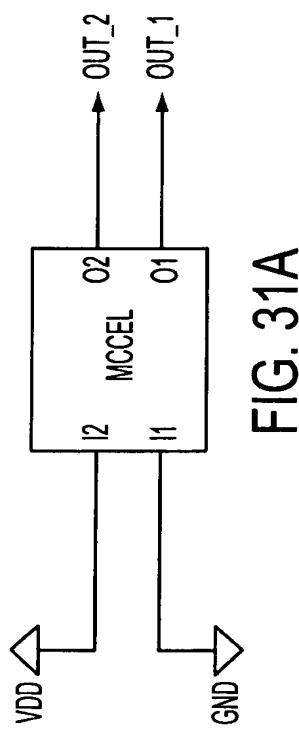


FIG. 31A

OUT_1	OUT_2	COMMENT
0	1	DEFAULT
1	0	METAL/VIA CHANGE

FIG. 31B

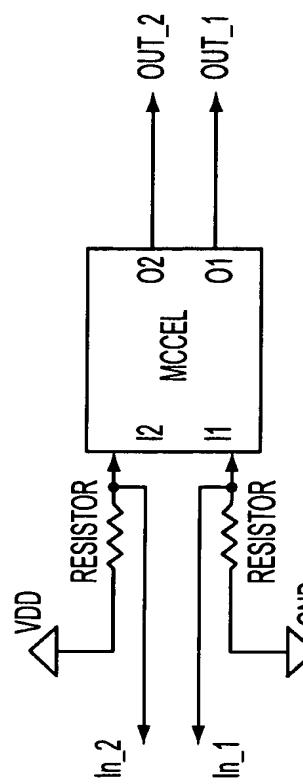


FIG. 31C

OUT_1	OUT_2	COMMENT
WEAK '0'	WEAK '1'	DEFAULT (In_1 & In_2 FLOATING)
WEAK '1'	WEAK '0'	METAL/VIA CHANGE (In_1 & In_2 FLOATING)

OUT_1	OUT_2	COMMENT
in_2	in_1	DEFAULT (In_1 & In_2 DRIVEN)
in_1	in_2	METAL/VIA CHANGE (In_1 & In_2 DRIVEN)

FIG. 31D

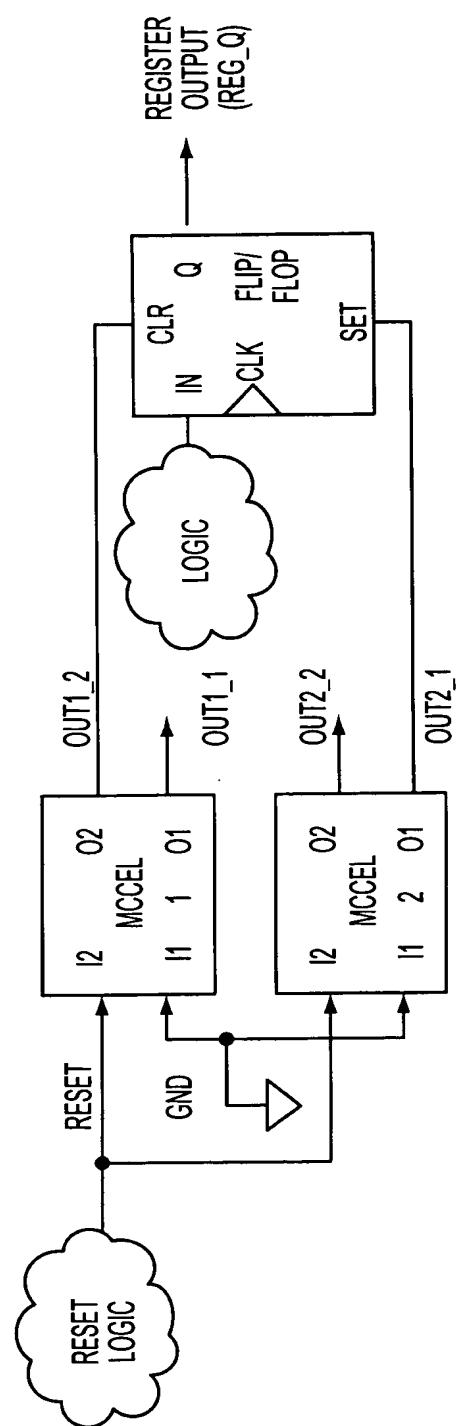


FIG. 32A

RESET	MCCEL1	MCCEL2	REG_Q
0	0	0	000000XX1
0000	00110011	01010101	
1111	11001100	10101010	

FIG. 32B

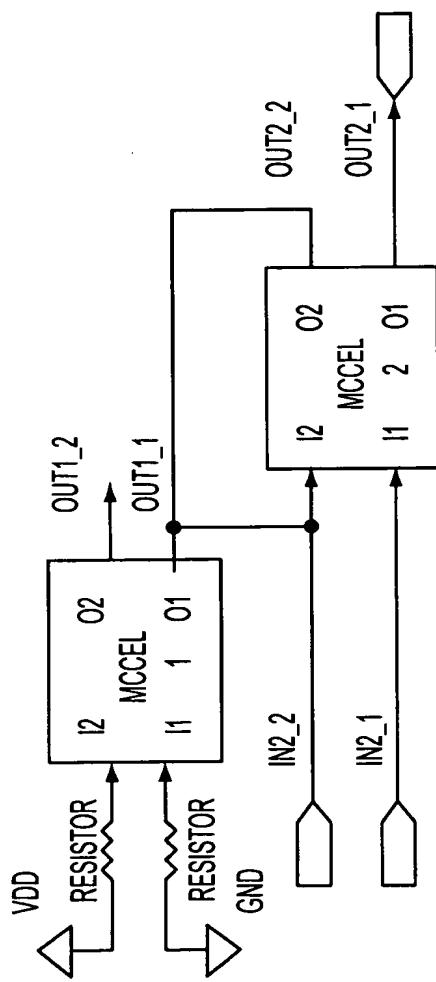


FIG. 33A

MCCEL1	MCCEL2	OUT2_1
0	0	IN2_1 (DEFAULT)
0	1	IN2_1 + IN2_2 + PULL-DOWN
1	0	IN2_1
1	1	IN2_1 + IN2_2 + PULL-UP

FIG. 33B

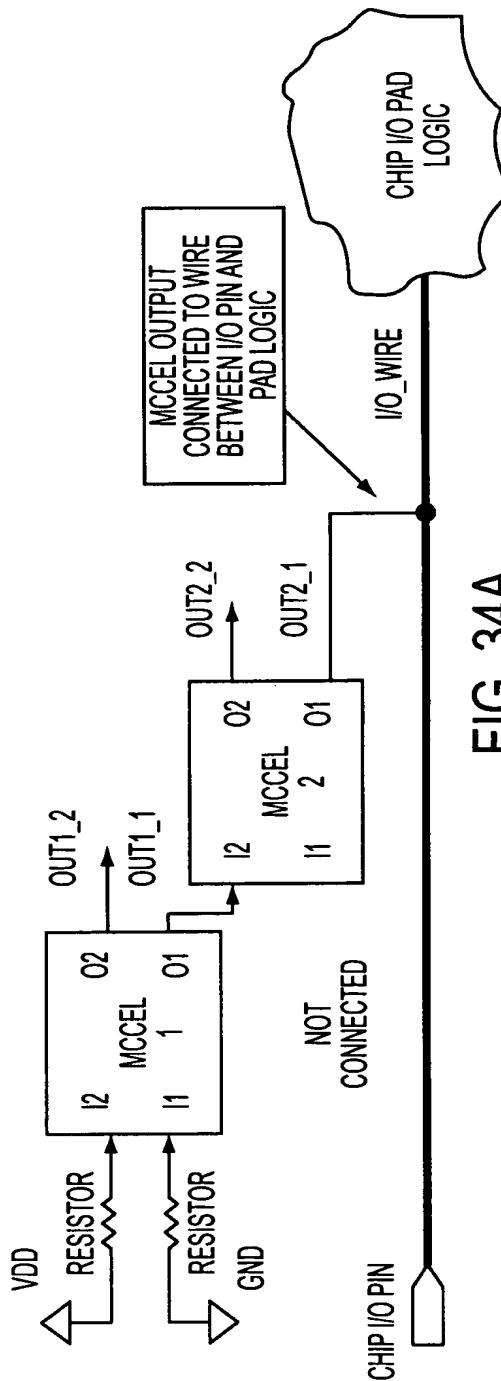


FIG. 34A

MCCEL1	MCCEL2	I/O PIN
0	0	I/O_WIRE (DEFAULT)
0	1	I/O_WIRE + PULL-DOWN
1	0	I/O_WIRE
1	1	I/O_WIRE + PULL-UP

FIG. 34B

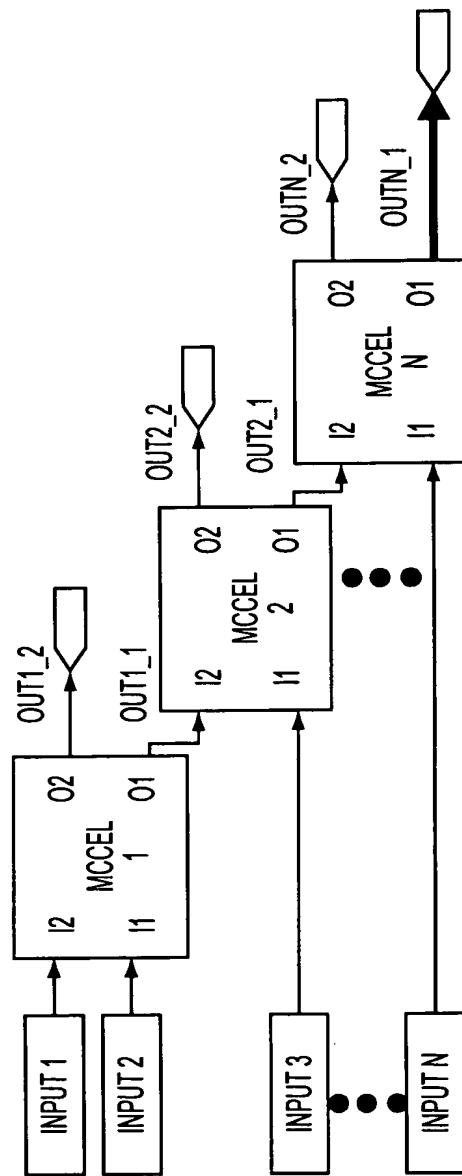


FIG. 35

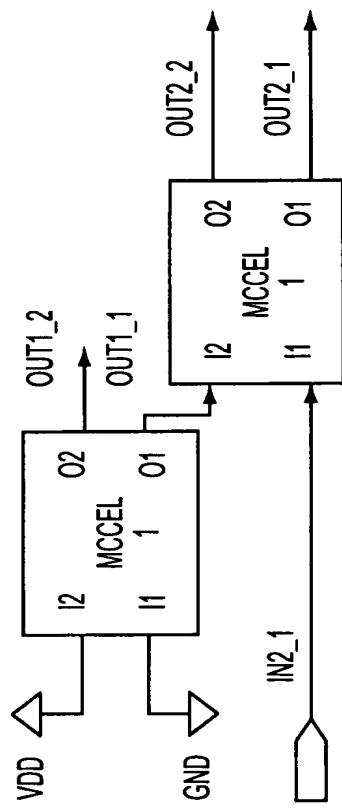


FIG. 36A

MCCEL1	MCCEL1	OUT2_1	OUT2_2
0	0	IN2_1 (DEFAULT)	0 (DEFAULT)
0	1	0	IN2_1
1	0	IN2_1	1
1	1	1	IN2_1

FIG. 36B

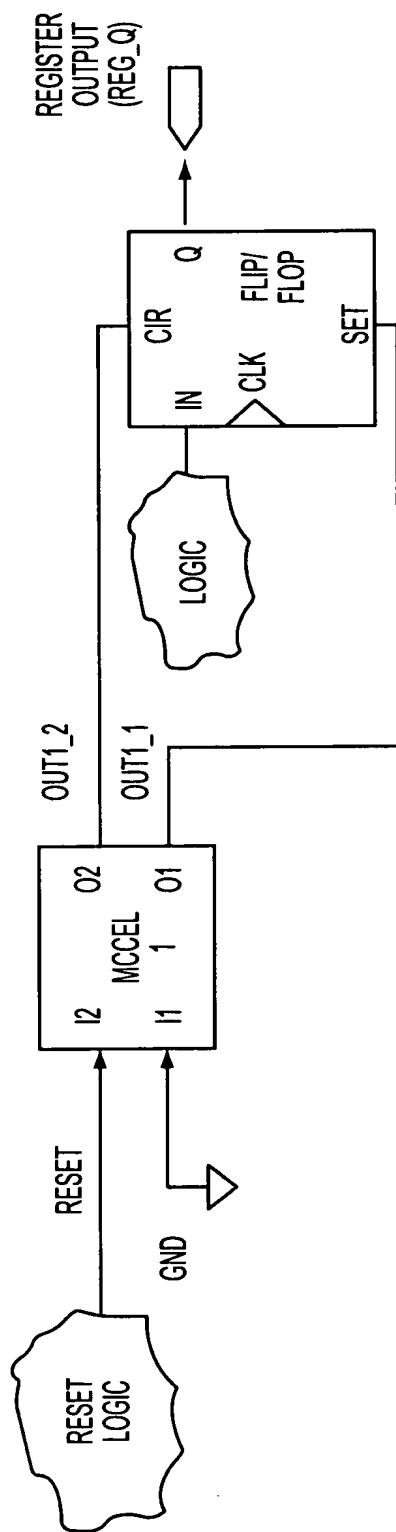


FIG. 37A

RESET	MCCEL1	REG Q
0	0	0
0	1	0
1	1	1

FIG. 37B